Driving the Gate of a EPC Space Rad Hard eGaN® HEMT Transistor

Introduction

High reliability, radiation-tolerant eGaN HEMT devices represent an exciting development for the space circuit design community. The transistors offer the designer a vastly improved $C_{ISS} \cdot R_{DS(on)}$ figure-of-merit (FOM) as well as much faster switching times when compared to conventional silicon MOSFETs. However, being a new technology, there are still some "institutional" concerns about this technology. The primary area of concern for the designer new to this technology in the application of a rad hard eGaN HEMT transistor is its limited gate-source voltage operating range as compared to that of familiar silicon MOSFET devices. For example, all available discrete-packaged EPC Space eGaN HEMT devices have a gate voltage range of +6 to -4 V, with +5 V being the optimum ON-state drive level. This compares to the +/-20 V range, and a +12 V optimum ON-state drive level, for a conventional rad hard, non-logic-level silicon MOSFET. Making this situation more complicated is the fact that full enhancement of the eGaN HEMT device (and the corresponding maximum current carrying operating point) is not achieved until a gate-source potential of approximately +4.2 V. Many designers will design to the typical data sheet transfer curves in regards to V_{GS} versus I_D. But this practice discounts the effects of aging, temperature, processing, parameter variations such as with transconductance, and the operating stresses presented to the device during its lifetime.

The RIGHT Gate-Source Voltage

Often the question *"the data sheet shows that the HEMT is saturated with 3.5 V of gate-source drive, how come EPC Space recommends 4.2 V drive, minimum, and a preferred level of 5.0 V?"* is asked by end-use designers. The reason for this difference is that EPC Space is in the business of producing high-reliability, rad hard eGaN HEMTs and as such we want the end-use designer to get the maximum benefit both in performance and reliability out of the application of a particular device. We consider our eGaN HEMT devices to be power switches and do not recommend linear mode operation. And our years of experience in the high-reliability, rad hard venue with regard to eGaN HEMTs has caused us to take the conservative approach to driving their gates – rather than applying a potential that might effectively saturate the device, causing application efficiency loss due to the resulting $\Delta R_{DS(on)}$ increase over life, etc., we recommend that half-measures of gate drive are abandoned in favor of the level that will give the best chance of a successful application outcome. A reasonable designer might ask, "*What about the losses incurred by the gate at the higher V_{GS} operating point?*"

EPC Space's answer to this is to consider the power dissipation at, say, 4.2 V and a gate leakage current of 1 mA. This is 4.2 mW of power dissipation. And we must also consider the additional AC losses due to the greater voltage level (from 3.5 V) or $P_{GATE(AC)} = C_{ISS} \cdot (4.22 - 3.52) \cdot f_s$, and furthermore assuming the device operates at 1MHz, this loss is $1000 \cdot 10^{-12} \cdot 5.39 \cdot 10^6$ for a typical device, or a 5.4 mW. The combined differential loss, assuming NO DC gate loss at 3.5 V is 9.6 mW. Now consider the HEMT operating at a V_{GS} of 3.5 V whose $R_{DS(on)}$ might vary 1-2 mΩ over life, etc. at that operating point. The losses incurred for such a deviation are proportional to $I_{D2} \cdot \Delta R_{DS(on)}$. Now consider this same device operating at a drain current of 10 A with the 2 mΩ incremental increase in ON resistance. This results in a 200 mW increase in the device's power dissipation just from this "under-drive" situation alone, or an over 20 times increase in power dissipation over just increasing the gate drive potential to 4.2 V. If one considers the consequences, moving to at least the 4.2 V drive level (despite the now-antiquated strictures to properly de-rate) is a no-brainer!

Now, at the flip side of the minimum gate drive requirement is the absolute maximum gate drive potential. As was previously mentioned, EPC Space specifies the maximum gate-source voltage as +6.0 V_{DC}. The reason that this stricture exists is that it is essential to not exceed the maximum (or minimum)

gate-source voltage because catastrophic damage may be done to the gate over time by this voltage over-stress. While it is tempting to think of this maximum voltage restriction can be explained by the breakdown characteristic of the gate-source junction, as shown in Figure 1, the reason is not that simple. Figure 1 shows the gate-source current (I_{GSS}) for the various EPC Space discrete product offerings for different V_{DS} breakdown voltages. Although an eGaN HEMT may be destroyed by dissipating excessive power in a single catastrophic over-voltage event (the gate source junction may be thought of as a voltage-offset metal-semiconductor junction, similar to a Schottky junction), irreparable damage to the gate structure of an eGaN HEMT is done by repeated voltage overstresses of any duration.

Even small excursions in gate voltage beyond the +6 V rating will yield ratcheting larger currents to be drawn by the gate, depending upon the device characteristics. The destructive process occurs as a result of the energy supplied to the gate as a result of the uncontrolled transient. The point at which each device will fail due to over-voltage insult to the gate will be dependent upon the physical size of the die (determining the thermal resistance), the internal gate series resistance and any minor imperfections in the gate-source/drain structure, and of course the magnitude, frequency, duration and total number of insults. The repeated voltage overstress events essentially damage the gate structure in a “death by a thousand cuts” manner. Eventually, because of this increased current drawn by the gate, the gate will experience what amounts to a death spiral of increasing gate current along with the excessive gate-related power dissipation, and the HEMT will catastrophically fail.

Consequently, it may seem like the designer does not seem to have much room for error in applying and properly driving HEMT devices! However, device packaging and a careful design approach eliminates all these gate drive concerns.

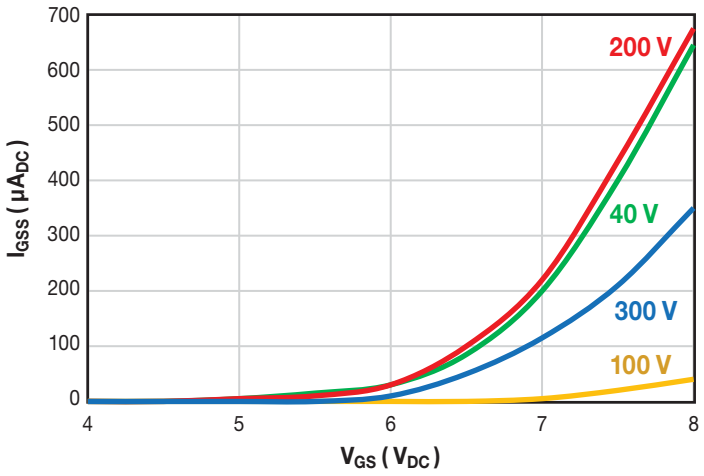


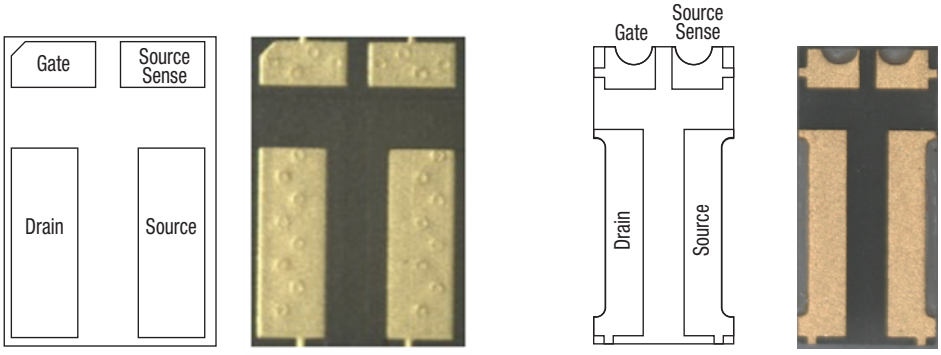
Figure 1: Typical EPC Space eGaN HEMT Gate-Source Forward Breakdown Characteristic

The Essential SOURCE SENSE Connection

The sensitivity of the eGaN HEMT to gate-source over-voltages requires that the designer be mindful of the accuracy/tolerance of the bias level of the power supply that provisions the gate driver. The designer MUST additionally insure that under all transient switching conditions that the gate-source potential is never allowed to exceed +6 V peak during switching transients.

To this end, the packaging for the EPC Space discrete eGaN HEMT and die products have been optimized to assist the designer in minimizing ringing and other transients due to gate/drain current interactions resulting from parasitic inductances.

For example, the I/O pads on the EPC Space FSMD-B SMT package are shown in Figure 2a and on the CDA die adapter package in Figure 2b. Each EPC Space SMT or die adapter package provides four separate I/O pad connections to the eGaN HEMT within: Gate, Source Sense, Drain and Source. The ‘Source Sense’ pad adjacent to the ‘Gate’ pad enables the designer to optimize the gate drive loop independently of the high current drain-source output loop, as shown in Figure 3b. The Source Sense pad is connected directly to the source on the die internal to the package – a true Kelvin connection, thus eliminating deleterious load current and gate current interactions. Internal to the package the Source and Source Sense pads have the same reference potential, that of the Source of the internal eGaN HEMT transistor.



(Bottom views)

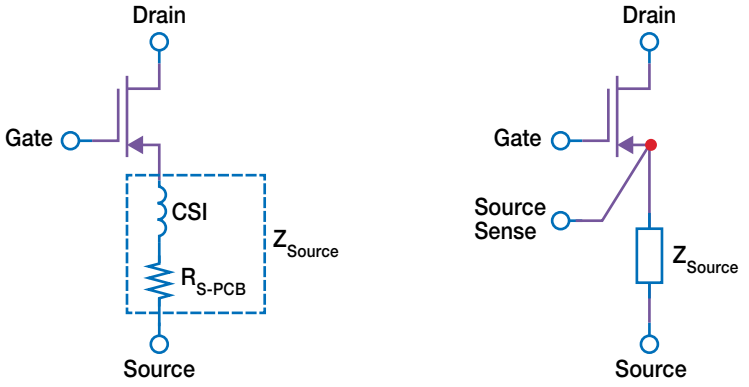
(a) EPC Space FSMD-B

(Bottom views)

(b) EPC Space CDA Package

Figure 2: EPC Space Discrete eGaN HEMT Packaging

An immediate benefit to the designer is that the high current, high di/dt drain current cannot influence the transient-sensitive gate current loop due to external (to the package) parasitic inductances and resistances in series with the high current source terminal (Z_{Source} in Figure 3a.). During current commutation, common power source inductance (CSI) is separated from gate return preventing the voltage induced by dI_D/dt (which even for very small parasitic inductances may be great due to the very high switching times of eGaN HEMTs) across the power source inductance present from being subtracted (added) from (to) the gate drive voltage during turn on (off), as shown in Figure 3a. Source inductance common to the gate drive and power loops (common source inductance or CSI) is a major contributor to losses and erratic operation during current commutation. thus eliminating deleterious load current and gate current interactions. Internal to the package the Source and Source Sense pads have the same reference potential, that of the Source of the internal eGaN HEMT transistor.



(a) **HEMT without** Source Sense Connection

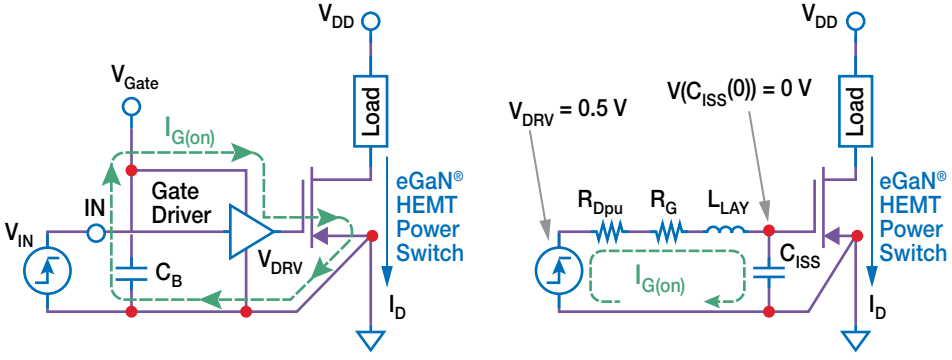
(b) **HEMT with** Source Sense Connection

Figure 3: EPC Space Source Sense Connection

Turning the eGaN HEMT On and OFF

However, just providing the Source Sense pad on the EPC Space SMT packages is not enough to prevent harmful transient voltages from appearing at the Gate terminal of the HEMT device. The most important consideration for reducing or eliminating voltage overshoot in the gate current loop during device turn-on is to reduce the parasitic inductance in the gate current loop that will affect the gate turn-on current, I_G(on), shown by the green arrows in Figure 4. The total loop area of this high transient current path determines, in large part, the parasitic inductance present in this current loop. In the equivalent turn-on circuit in Figure 4b., it can be clearly seen that the gate driver pull-up resistance (R_{Dpu}) and the HEMT gate resistance (R_G), the loop inductance (L_{LAY}) and the input capacitance (Ciss) form a series R-L-C resonance circuit. In the equivalent circuit, R_{Dpu} is the pull-up resistance of the gate driver, R_G is the internal gate resistance of the HEMT and C_{ISS} the gate-source input capacitance of the HEMT.

The quantities/parameters R_{Dpu}, R_G and C_{ISS} are all fixed for a given circuit design and the components selected – they are data sheet parameters for the HEMT and the gate driver, so the principal goal for the designer is therefore to keep L_{LAYOUT} as small as possible by making the connections from the output of the gate driver to the HEMT gate, from the power input of the gate driver to the gate driver power supply bypass capacitor (C_B) and from the Source Sense pad to the power supply bypass capacitor as short as possible, and, if possible, route gate drive and return paths on separate board layers over each other to cancel inductances. It is recommended that the Source Sense connection in the gate loop be implemented as a small copper etch area on the PCB, and not just an etch trace. This implementation mimics, on a smaller scale, the properties of a ground plane. The gate power supply bypass capacitor should be located and connected directly across the power supply and ground pins of the gate driver IC – or as close as possible to the high current driver elements of a discrete gate driver circuit. The connection from the output from the gate driver should be as short as practicably possible. The width of this connection should be at least one-half of the length in order to minimize unwanted parasitic/passive elements.



(a) HEMT/gate driver during turn-ON

(b) Equivalent circuit including parasitic elements at turn-ON

Figure 4: eGaN HEMT at Turn-ON

In reality, it is practically impossible to reduce the loop area enough to prevent unwanted loop inductance. This might happen because of proximity limitations due to component sizes or printed circuit board mechanical restrictions, or simply because of parasitic inductances in component packages. Figure 5 shows the PSPICE simulation output for the gate-source voltage of a FBG10N30B eGaN HEMT (R_G = 0.6 Ω and C_{ISS} = 700 pF) with a gate driver pull up resistance of 2 Ω and with series inductance values (L_{LAY} in Figure 4b.) ranging from 1 nH to 20 nH in 1 nH steps. It is clear that for series inductance values up to approximately 7.5 nH, the gate voltage does not exceed the absolute maximum value of +6 V. A close-up of the gate-source voltage for inductance values up to 7.5 nH is shown in Figure 6, proving that the gate-source voltage does not exceed +6 V.

Now, for the larger values of series inductance unavoidably present in the gate circuit, all is not lost, as the designer has a valuable option to use to reduce the magnitude of the parasitic resonance peak voltage: damping resistance. This damping resistance (R_D) should be placed in series with the output of the gate driver and the HEMT gate. The total series resistance in the gate circuit becomes R_{Dpu} + R_G + R_D. For example, Figure 7 shows the gate voltage simulation results for the case of 1 to 20 nH of series inductance with an added damping resistance value of 2 Ω. It can be seen in Figure 7 that even to the maximum 20 nH inductance level that the gate-source voltage does not exceed the +6 V maximum rating of the device. These results demonstrate the value and effectiveness of the judiciously-chosen, additional gate damping resistance.

Caution must be exercised in applying the damping resistance as when the value is increased, the peak available gate current is limited, and the rise and fall times of the gate voltage are increased. The net effect is a decrease in the overall performance of the circuit – for example a decrease in conversion efficiency in a power supply. So, the designer must keep the damping resistance to the lowest reasonable value that balances the gate switching performance desired and the maximum peak gate voltage allowed or desired. If an integrated or discrete driver is used that has separate gate pull-up and pull-down outputs, it is recommended that the damping resistance be utilized in the gate pull-up output only, as ratings-threatening overshoots in gate voltage will be encountered during and affect only the turn-on event. This implementation allows the switching performance of the eGaN HEMT to be maximized in that the performance of the turn-on loop is only, necessarily, affected by the required damping and the turn off loop remains optimized to pull the gate to the source with the lowest resistance possible, and thus providing for the fastest gate turn-off time possible.

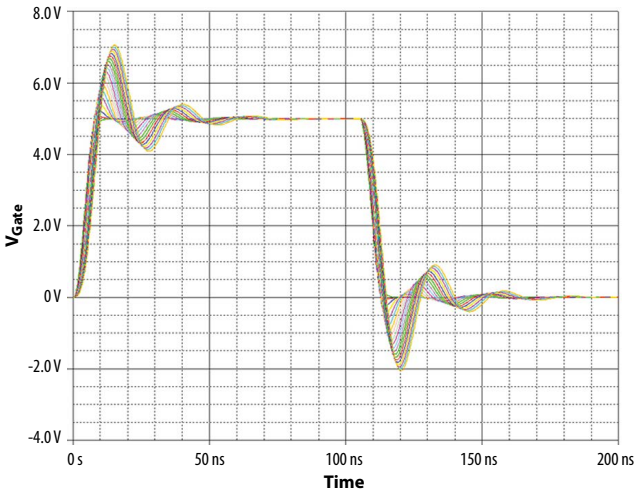


Figure 5: EPC Space eGaN HEMT Gate-Source Voltage Simulation: Series Inductance From 1nH to 20 nH

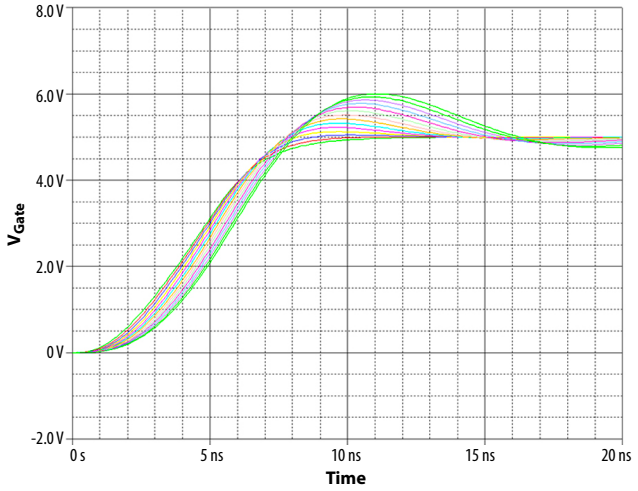


Figure 6: EPC Space eGaN HEMT Gate-Source Voltage Simulation: Series Inductance From 1nH to 7.5 nH (Close-Up)

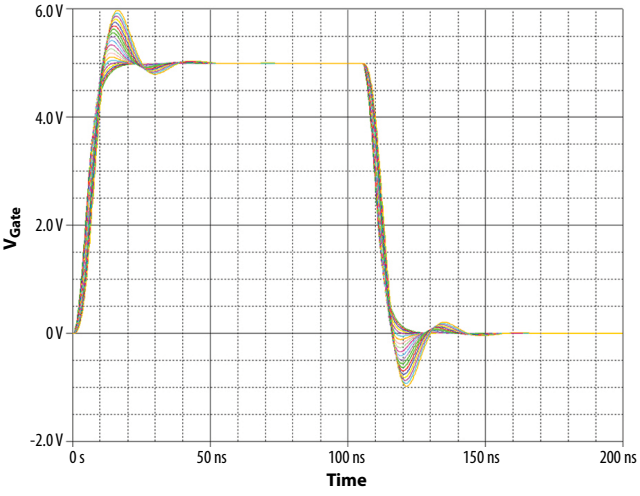
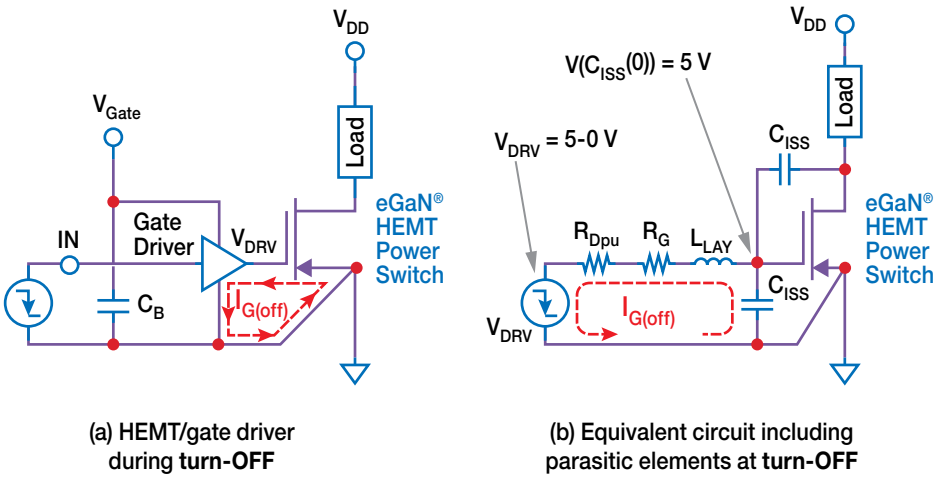


Figure 7: EPC Space eGaN HEMT Gate-Source Voltage Simulation: Series Inductance From 1nH to 20 nH (2 Ω damping resistance).

The turn-off circuit for the eGaN HEMT is shown in Figure 8. It is similar to the turn-on circuit shown in Figure 4 with the exception that the gate driver output resistance is R_{Dpd} – the driver pull-down resistance. For integrated gate drivers, the pull-up and pull-down resistances are often different, with the pull-down resistance lower than the pull-up resistance. This will not be a problem in terms of the peak transient undershoot of the gate-source voltage at turn-off because the voltage margin from 0 V (the final gate turn-off potential) to the absolute maximum value of -4 V is four times that of the margin between the optimum gate drive voltage (+5 V) and the absolute maximum rating of +6 V, or 1 V margin. Also, the lower pull-down resistance value helps to ensure that the HEMT gate will remain below the gate-source threshold voltage ($V_{GS(th)}$) even with the effects of the Miller capacitance (C_{RSS}) accounted for. Although the rate-of-change of drain voltage can be considerable (for example 100 V in 10 ns for the FBG10N30, or 10,000 V/µs), the value of Crss for the eGaN HEMTs is small in comparison to conventional MOSFETs (for the FBG10N30, C_{ISS} = 30 pF).

For example, Figure 9 shows the PSPICE simulation for the equivalent circuit shown in Figure 8b. for an FBG10N30 with a pull-down resistance of 2 Ω, no damping resistance and the layout inductance L_{LAY} varied from 1 nH to 20 nH.

It can be seen that for all values of inductance that gate-source voltage remains below the minimum gate-source voltage threshold for the FBG10N30 of 0.8 V. However, this is the 25°C value, and at 125°C junction temperature the $V_{GS(th)}$ is 0.7 V, so gate-source voltage exceeds the minimum $V_{GS(th)}$ value for the three highest values of L_{LAY}, and there is a risk of transient dynamic turn-on at the HEMT turn-off event. In practice, this would not be a significant issue because at HEMT turn-off, the bypass capacitor (C_B) is excluded from the circuit, and this component carries with it a not inconsiderable inductance due to its physical side/length, and thus L_{LAY} during turn-off will be less that at turn-on due to its exclusion from the circuit.



(a) HEMT/gate driver during **turn-OFF**

(b) Equivalent circuit including parasitic elements at **turn-OFF**

Figure 8: eGaN HEMT at Turn-OFF

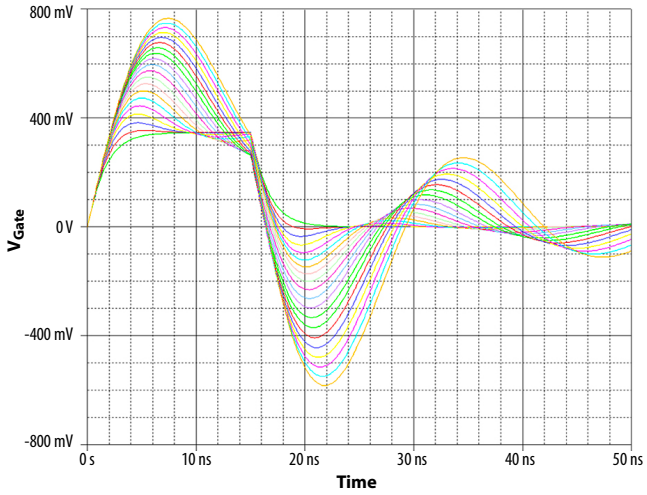


Figure 9: EPC Space eGaN HEMT Gate-Source Voltage Simulation: Series Inductance From 1nH to 20nH with Miller Feedback

Conclusion

EPC Space eGaN rad hard HEMTs represent a leap forward in electrical performance over conventional silicon rad hard MOSFETs. Recognizing and accommodating the device's ratings, particularly those relating to the gate-source input, will allow the designer to extract and enjoy all the benefits that these high-performance transistors offer. Recognizing that these transistors are not the same as silicon MOSFETs much in the same what when silicon MOSFETs were introduced that there were differences between them and silicon bipolar transistors is key in realizing the HEMT-to-MOSFET performance increases. The guidelines provided in this discussion allow the circuit designer to implement EPC Space eGaN HEMTs both efficiently and reliably, the most important criteria for space product design.