

Features

- Low $R_{DS(on)}$
- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
 - SEE immunity up to LET of 83.3 MeV/mg/cm² with V_{DS} up to 100% of rated Breakdown
- Neutron
 - Maintains Pre-Rad specification for up to 4×10^{15} Neutrons/cm²



EPC7003ASH

**Rad-Hard eGaN® 100 V, 10 A,
52 mΩ Surface Mount (FSMD-A)**

Description

EPC Space FSMD-A series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Applications

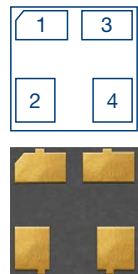
- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	10.6	

I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	SS	Source Sense
4	S	Source



Absolute Maximum Rating ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	100	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150°C)	120	
I_D	Continuous Drain Current I_D @ $V_{GS} = 5\text{ V}$	10	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} \leq 80\ \mu\text{s}$	38	
V_{GS}	Gate-to-Source Voltage (Note 2)	+6 / -4	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1A (ΔA)	
Weight	Device Weight	0.068	g

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	BV_{DSS}	$V_G = 0\text{ V}$	100			V
Drain to Source Leakage	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		1	60	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		10	150	
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 6\text{ V}$		1	300	μA
		$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		40	600	
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4\text{ V}$		0.07	60	
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 2\text{ mA}$	0.8	1.6	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}$			0.57		$\text{mV}/^\circ\text{C}$
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$I_D = 10\text{ A}, V_{GS} = 5\text{ V}$		42	52	$\text{m}\Omega$
Source to Drain Forward Voltage	V_{SD}	$I_S = 0.5\text{ A}, V_G = 0\text{ V}$		2	3	V

Dynamic Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		168	233	pF
Reverse transfer Capacitance	C_{RSS}			0.3	20	
Output Capacitance	C_{OSS}			92	170	
Total Gate Charge (Note 6)	Q_G	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 10\text{ A}$		1.8	2.2	nC
Gate-to-Source Charge (Note 6)	Q_{GD}			0.5	1.2	
Gate-to-Drain Charge (Note 6)	Q_{GS}			0.67	1	
Output Charge (Note 5)	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		8.5		
Source-Drain Recovery Charge (Note 5)	Q_{RR}	$I_D = 10\text{ A}, V_{DS} = 100\text{ V}$		0		

Radiation Characteristics

EPC Space eGaN[®] HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON	$V_{GS} = 5\text{ V}$
NO BIAS	$V_{DS} = V_{GS} = 0\text{ V}$
OFF	$V_{DS} = 80\% B_{VDSS}$

Electrical Characteristics up to 1000 krad ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	$V_{GS} = 0\text{ V}$	100			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 2\text{ mA}$	0.8	1.6	2.5	
Drain to Source Leakage	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		1	60	μA
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 5\text{ V}$		10	300	
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4\text{ V}$		0.07	60	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$I_D = 10\text{ A}, V_{GS} = 5\text{ V}$		42	52	$\text{m}\Omega$

Typical Single Event Effect Safe Operating Area

Note: All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M. The ion LET is based on the K-500 Cyclotron as it enters the device and is used as a reference to penetrating silicon devices.

Test	Environment				V_{DS} Voltage (V)	
	Ion	LET (in Si) $\text{MeV}/\text{mg}/\text{cm}^2$	Range μm	Energy MeV	$V_{GS} = 0\text{ V}$	$V_{GS} = -4\text{ V}$
See SOA	Xe	63	71.3	962	100	100
	Au	83.3	121	2256	100	100

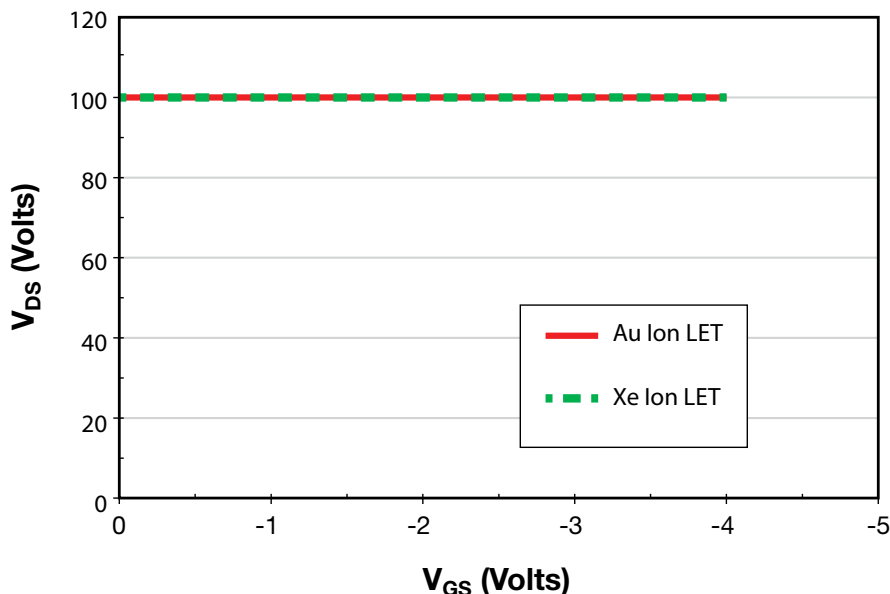


Figure 1. Typical Single Event Effect Safe Operating Area

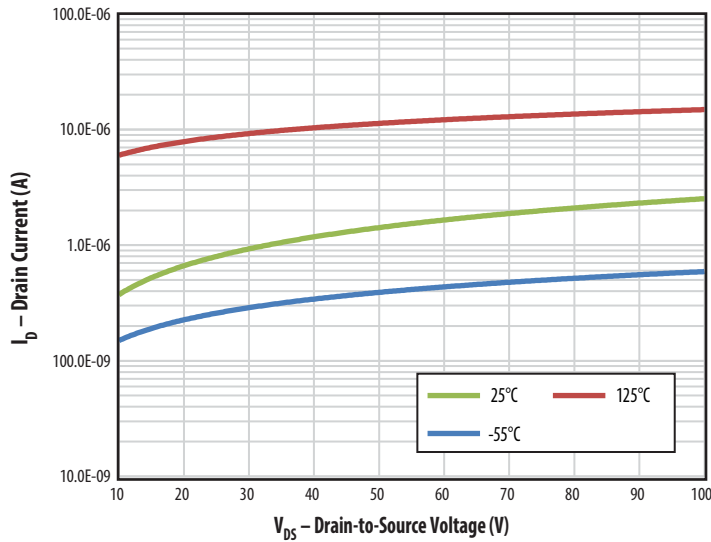


Figure 2. Typical Drain-Source Leakage Current vs. Ambient Temperature

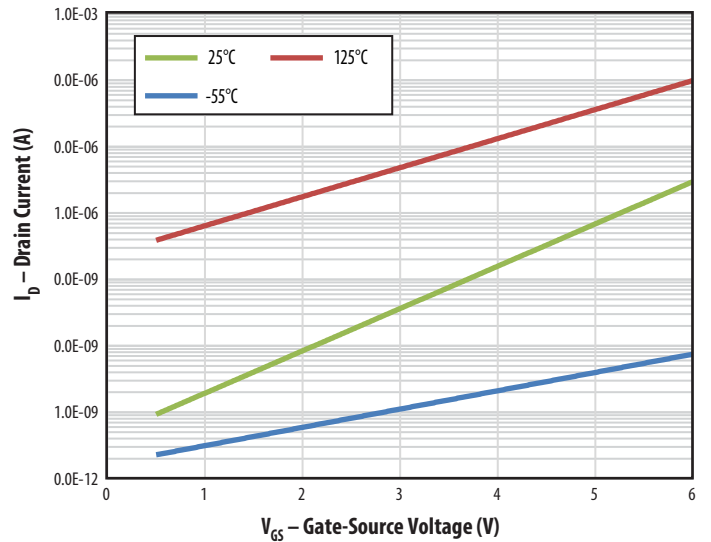


Figure 3. Typical Gate-Source Leakage Current vs. Ambient Temperature

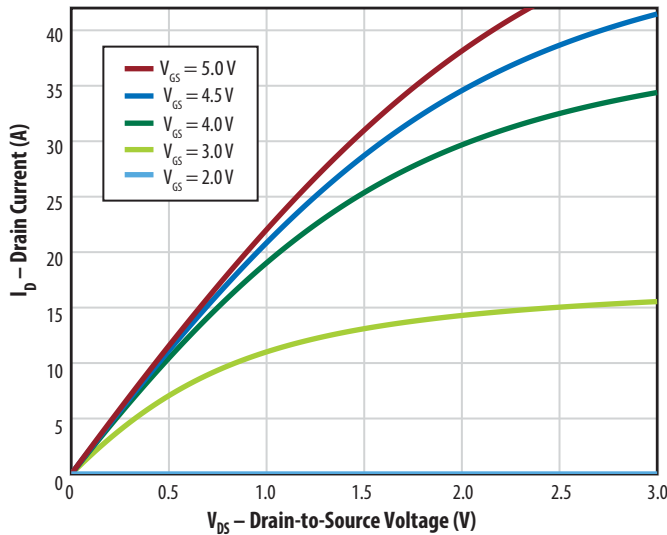


Figure 4. Typical Output Characteristics at 25°C

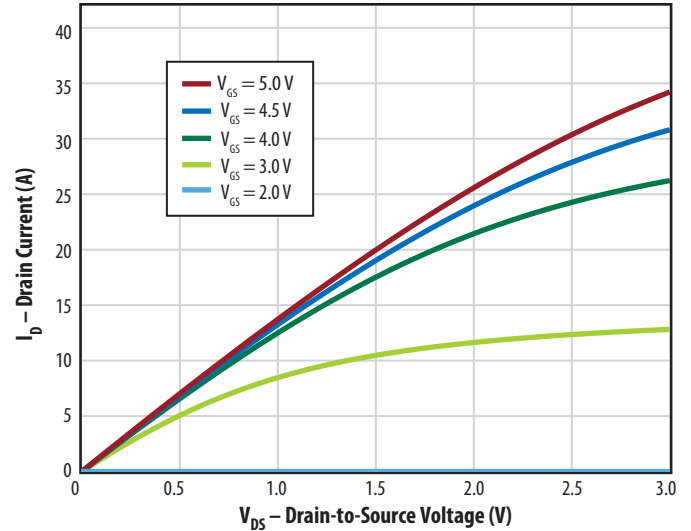


Figure 5. Typical Output Characteristics at 125°C

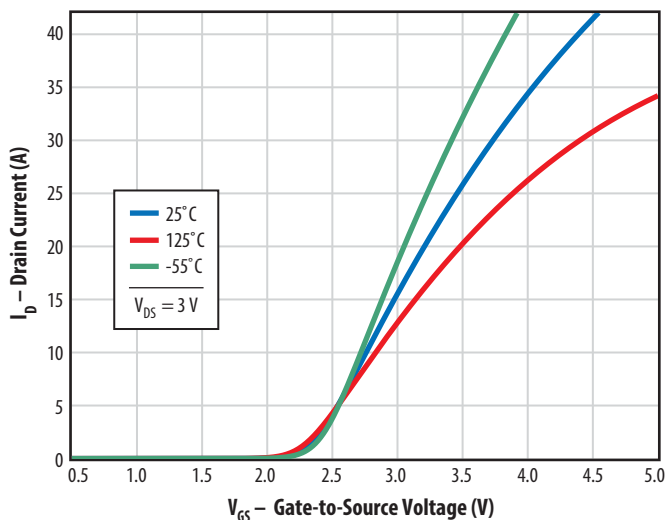


Figure 6. Typical Transfer Characteristics

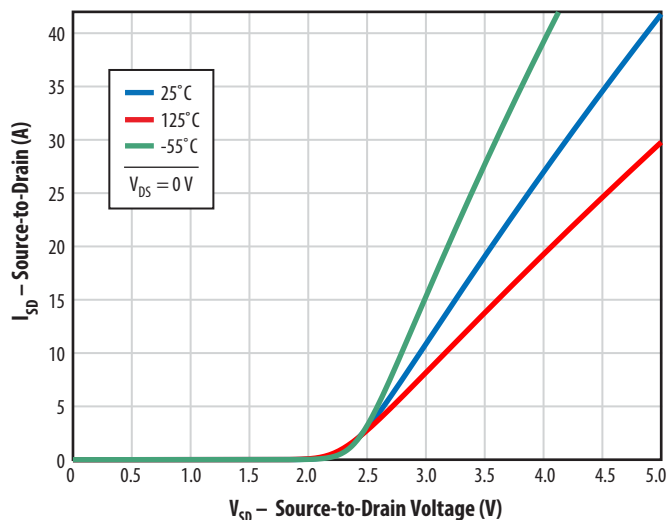


Figure 7: Reverse Drain-Source Characteristics

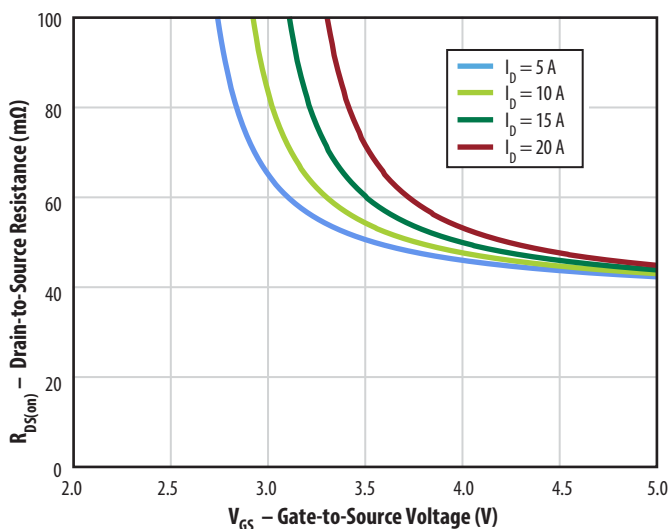


Figure 8. $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

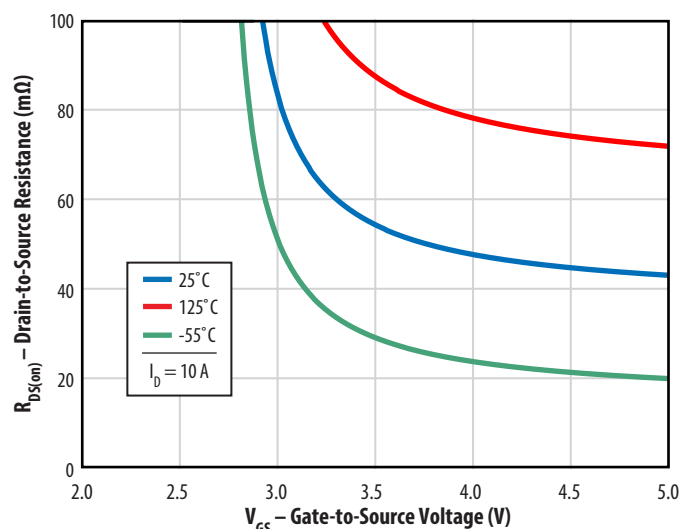


Figure 9. $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

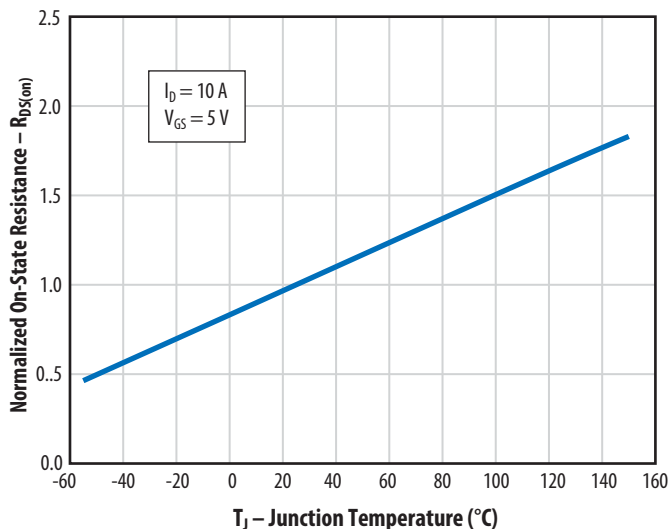


Figure 10. Normalized On-State Resistance vs. Temperature

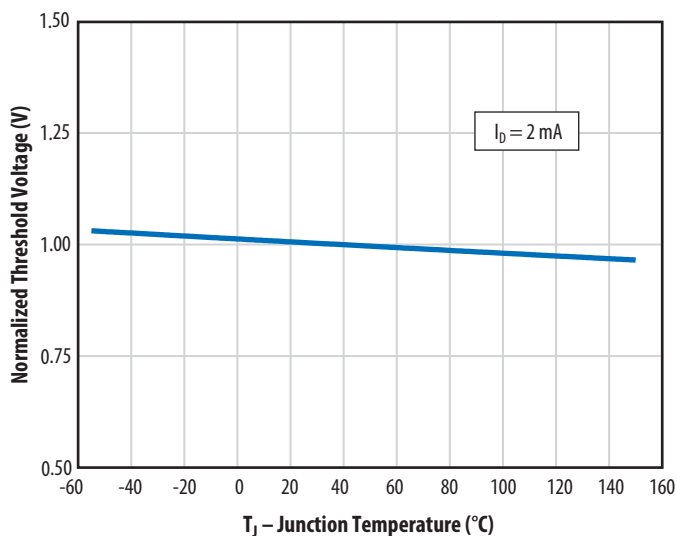


Figure 11. Normalized Threshold Voltage vs. Temperature

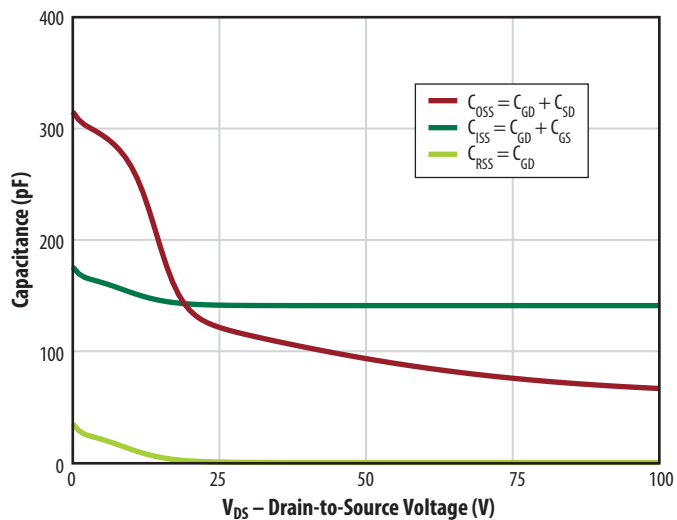


Figure 12. Typical Gate Charge

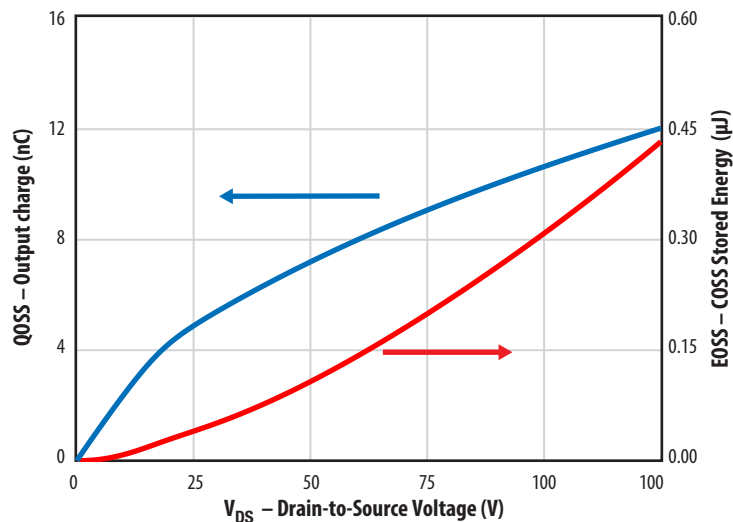


Figure 13. Typical Output Charge and C_{OSS} Stored Energy

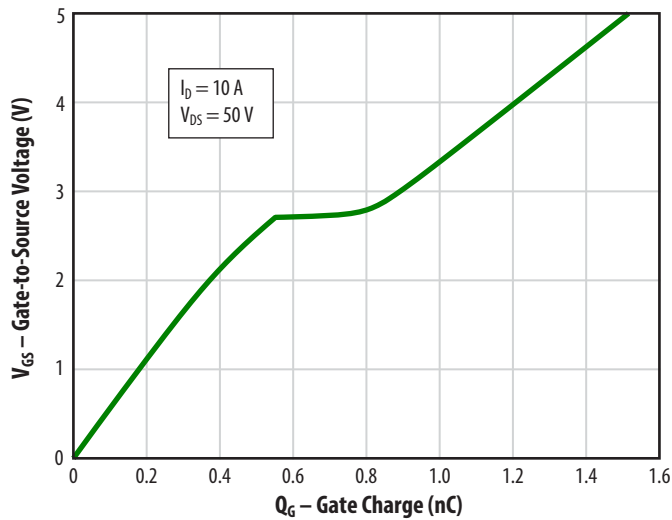


Figure 14. Typical Gate Charge

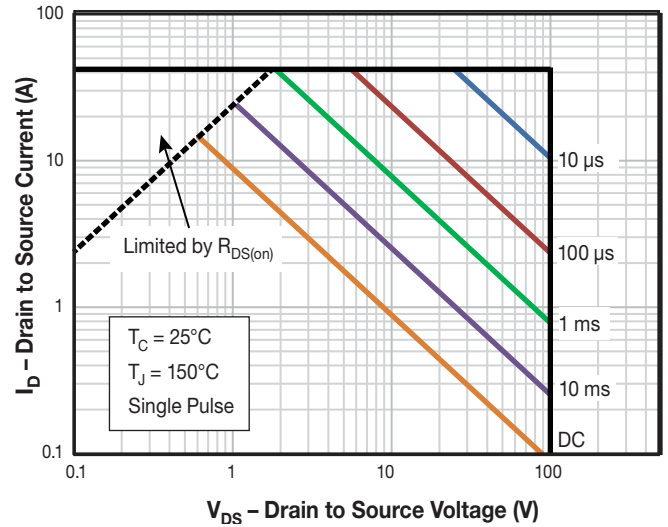


Figure 15. Safe Operating Area

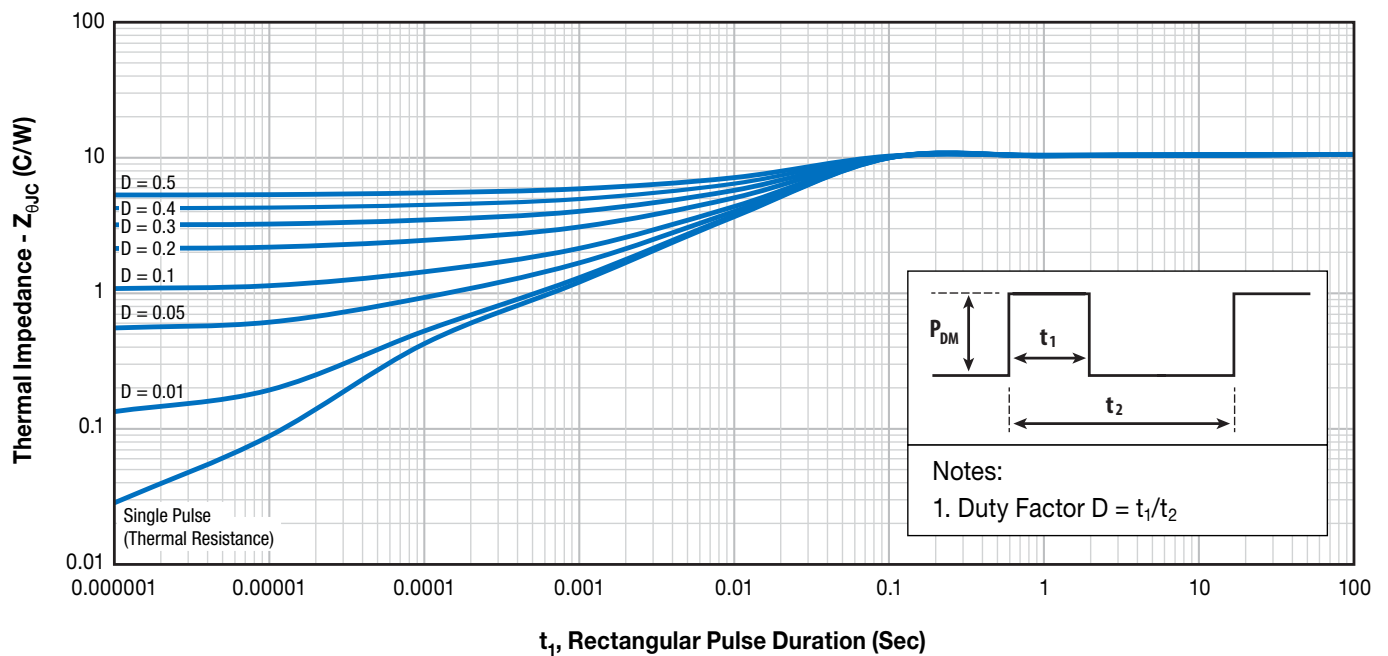
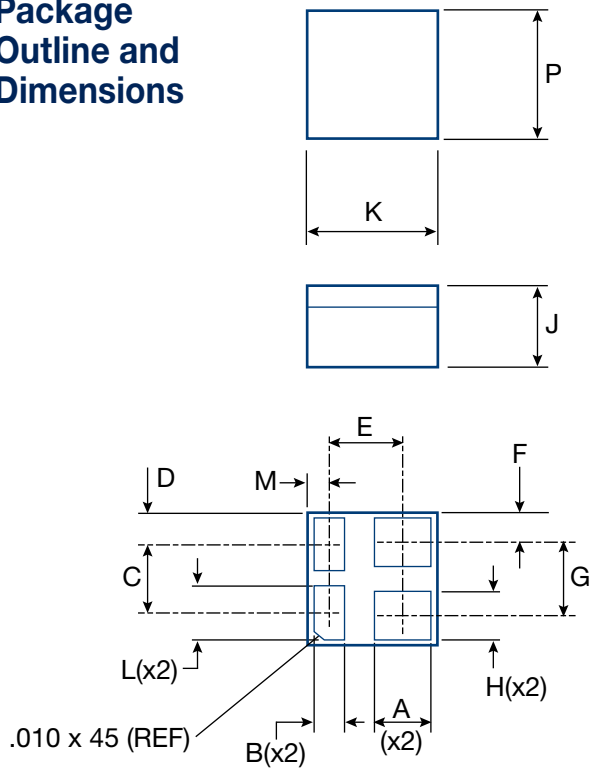


Figure 16. Transient Thermal Impedance, Junction to Case

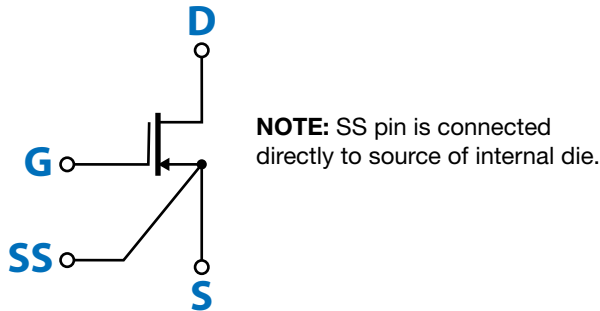
Package Outline and Dimensions



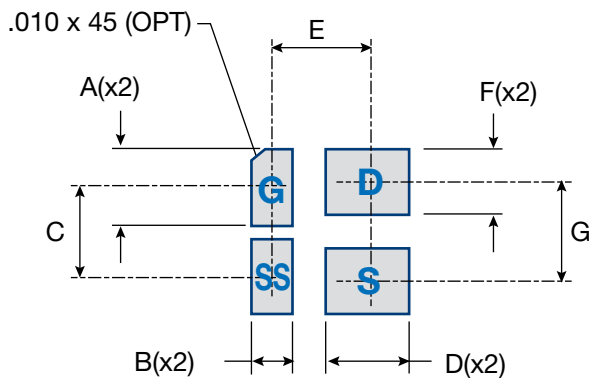
Symbol	Dimensions Nominal		Note
	in	mm	
A	0.062	1.57	
B	0.032	0.81	
C	0.068	1.73	
D	0.031	0.79	(REF)
E	0.074	1.88	
F	0.026	0.66	(REF)
G	0.076	1.93	
H	0.045	1.14	
J	0.083	2.11	(REF)
K	0.130	3.3	
L	0.053	1.35	
M	0.021	0.53	(REF)
P	0.130	3.3	

- Standard tolerances:
Length: $\pm 0.005''$ / $\pm 0.127\text{mm}$
- Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb.

Package Connections



FSMD-A Footprint for Printed Circuit Board Design



Symbol	Dimensions Nominal		Note
	in	mm	
A	0.057	1.45	
B	0.036	0.91	
C	0.063	1.6	
D	0.066	1.68	
E	0.074	1.88	
F	0.047	1.19	
G	0.076	1.93	

Notes

- Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.
- Note 3. $R_{\theta JA}$ measured with FSMD-A package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 μ s and duty cycle is 1%, maximum.
- Note 5. Guaranteed by design/device construction. Not tested.
- Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S . The gate current is adjusted to yield the desired charge per unit time ($I_{const} \cdot \text{time per division}$) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off}/t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC} .

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