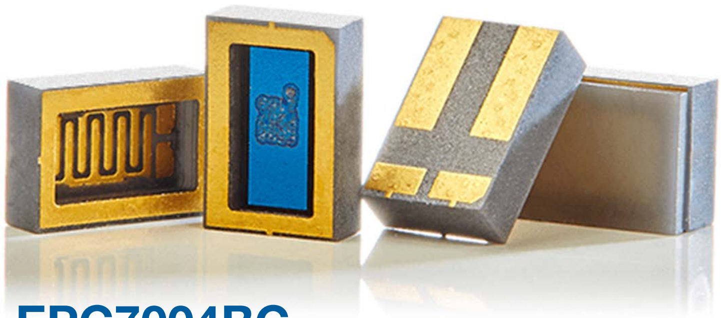
Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 85 MeV/mg/cm^2 with V_{DS} up to 100% of rated Breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 4 x 10^{15} Neutrons/cm^2

Applications

- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities



EPC7004BC

Rad-Hard eGaN® 100 V, 46 A,
16 mΩ typ Surface Mount (FSMD-B)

Description

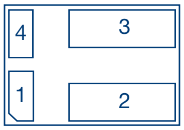
EPC Space FSMD-B series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	35	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	2.25	

I/O Pin Assignment *(Bottom View)*

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	SS	Source Sense



Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	100	V
I_D	Continuous Drain Current ID @ V_{GS} = 5 V, T_C = 25°C	46	A
I_{DM}	Single-Pulse Drain Current t_{pulse} ≤ 80 µs	160	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1A (ΔA)	
Weight	Device Weight	0.135	g

Electrical Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	V_{DSMAX}	V_G = 0 V	100			V
Drain to Source Leakage	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V		0.36	250	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_J = 125°C		3.1	500	
Gate to Source Forward Leakage	I_{GSSF}	V_{GS} = 5 V		10	500	
Gate to Source Forward Leakage		V_{GS} = 5 V, T_J = 125°C		20	1000	
Gate to Source Reverse Leakage	I_{GSSR}	V_{GS} = -4 V		0.36	250	
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 8 mA	0.8	1.4	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T$			|1.26|		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	V_{GS} = 5 V, I_D = 46 A		13	16	mΩ
Source to Drain Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 0.5 A		1.7	3	V

Dynamic Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 50 V, V_{GS} =0 V		797	1000	pF
Reverse transfer Capacitance	C_{RSS}			1.8	30	
Output Capacitance	C_{OSS}			411	700	
Effective Output Capacitance, Energy Related	$C_{OSS(ER)}$	V_{DS} = 0 to 50 V, V_{GS} =0 V		522		
Effective Output Capacitance, Time Related	$C_{OSS(TR)}$			690		
Total Gate Charge (Note 6)	Q_G	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 30 A		7	11	nC
Gate to Source Charge (Note 6)	Q_{GS}	V_{DS} = 50 V, I_D = 30 A		2.4	6	
Gate to Drain Charge (Note 6)	Q_{GD}			1.7	3	
Output Charge (Note 5)	Q_{OSS}	V_{DS} = 50 V, V_{GS} = 0 V		35		
Source to Drain Recovery Charge (Note 5)	Q_{RR}	I_D = 15 A, V_{DS} = 50 V		0		

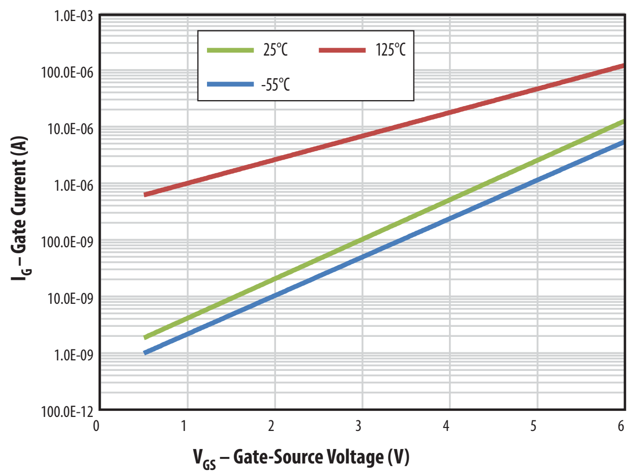


Figure 1. Typical Gate-Source Leakage Current vs. Ambient Temperature

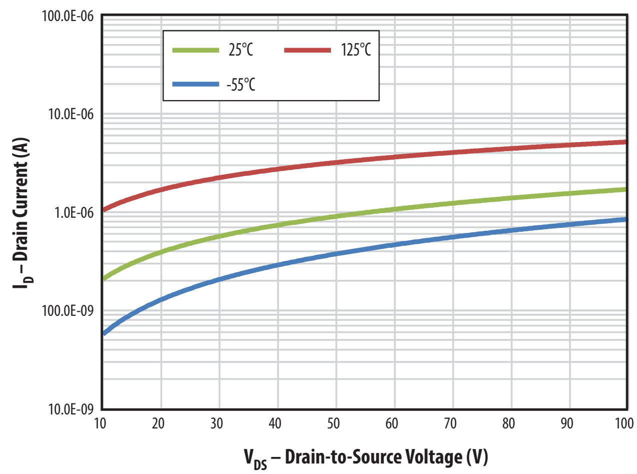


Figure 2: Typical Drain-Source Leakage Current vs. Ambient Temperature

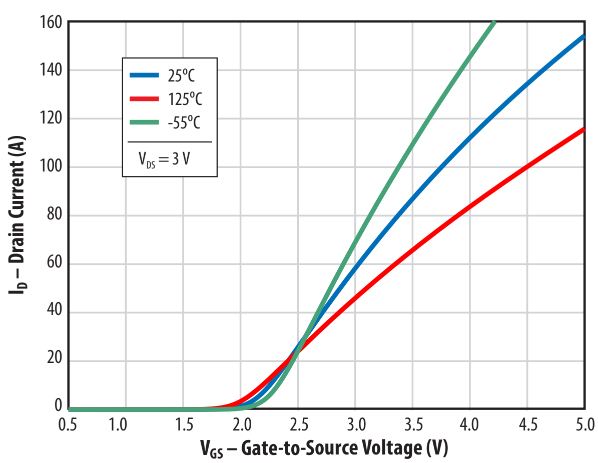


Figure 3. Typical Transfer Characteristics

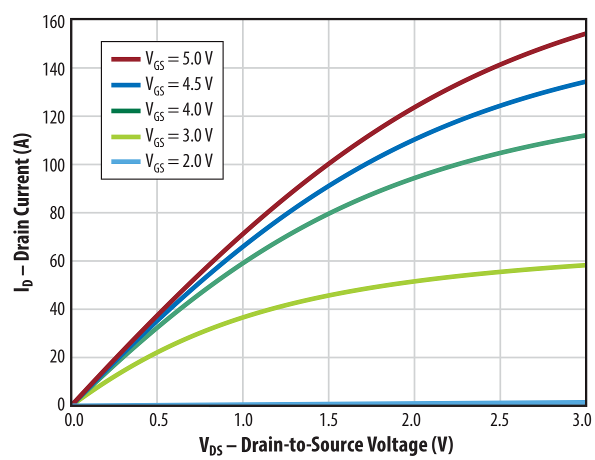


Figure 4. Typical Output Characteristics at 25°C

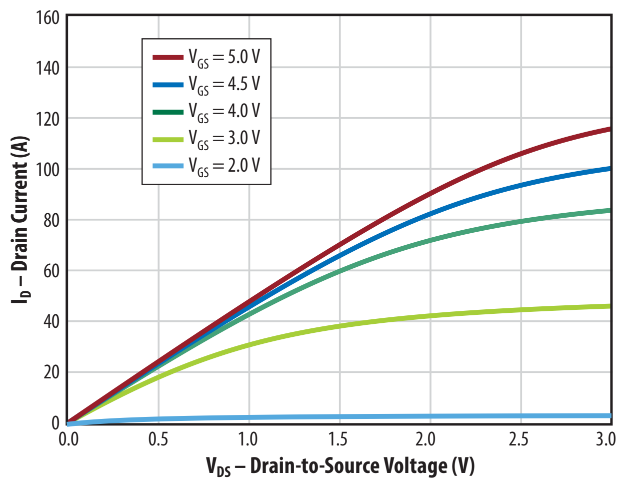


Figure 5. Typical Output Characteristics at 125°C

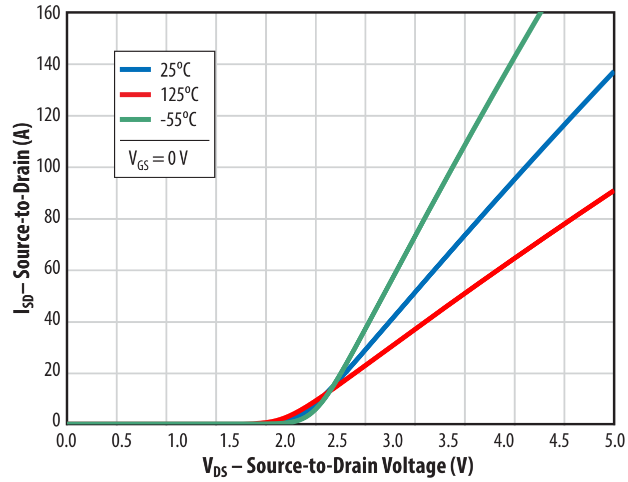


Figure 6. Reverse Drain-Source Characteristics

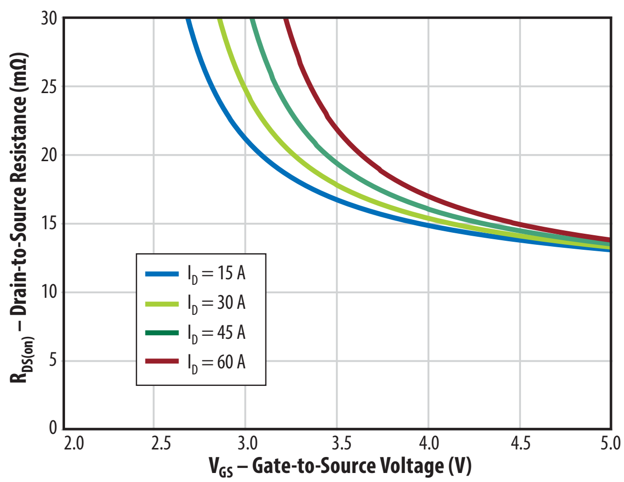


Figure 7. $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

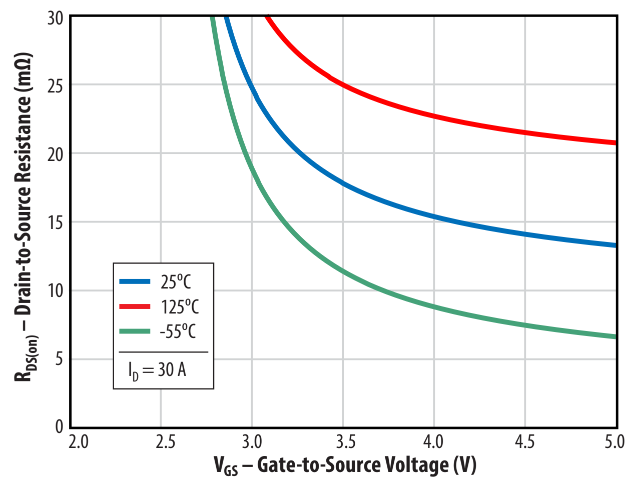


Figure 8. $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

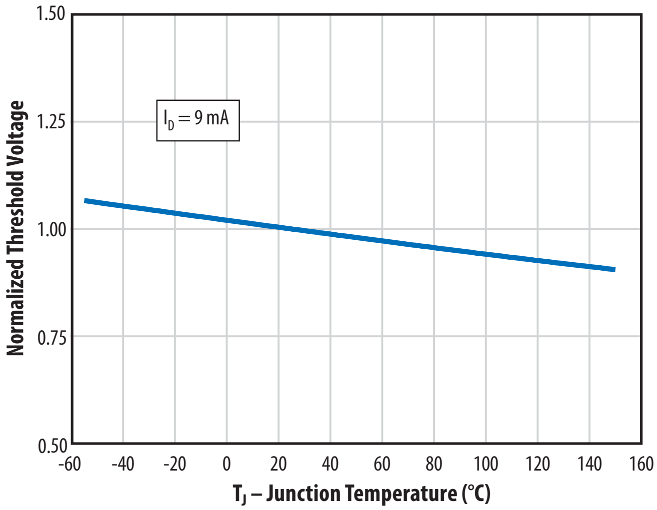


Figure 9. Normalized Threshold Voltage vs. Temperature

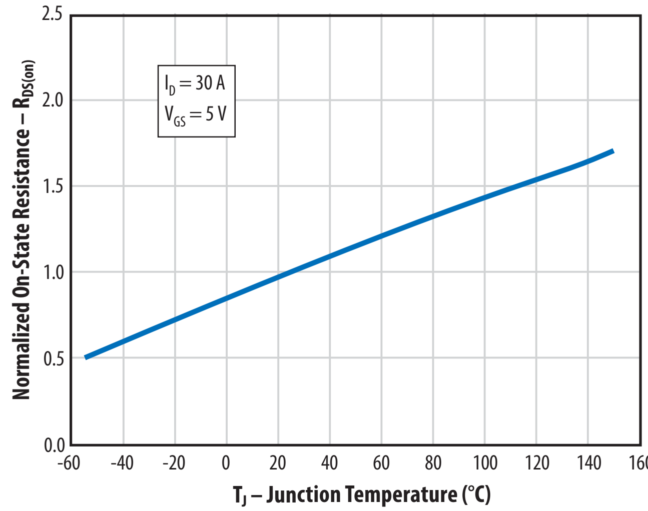


Figure 10. Normalized On-State Resistance vs. Temperature

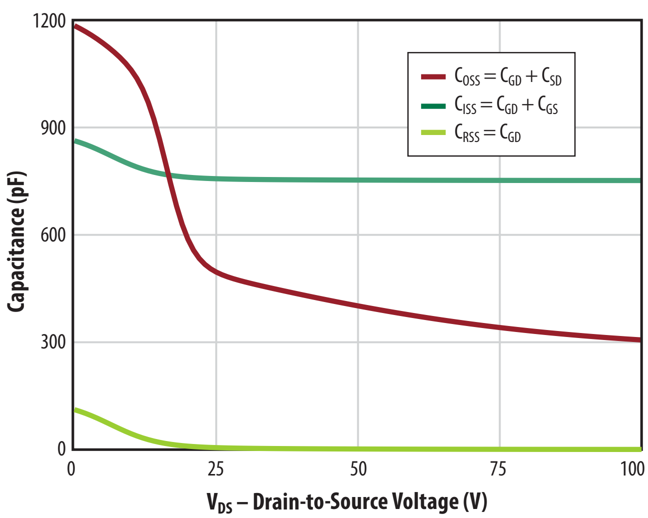


Figure 11. Typical Capacitance

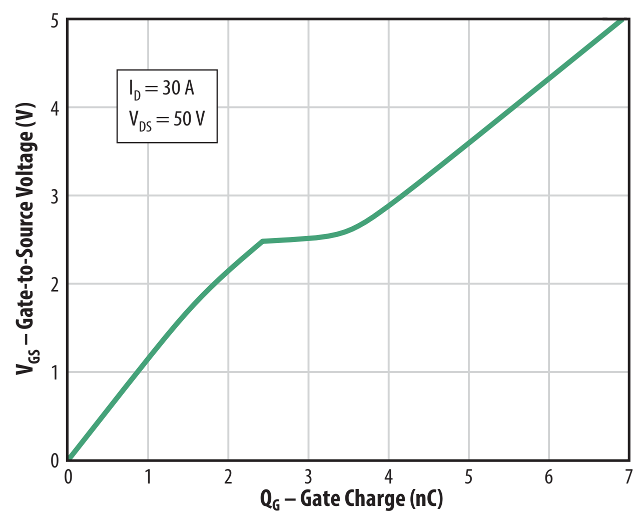


Figure 12. Typical Gate Charge

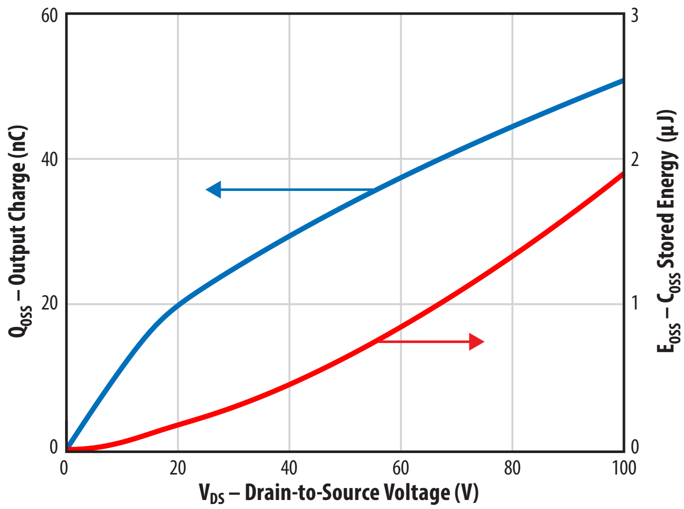


Figure 13. Typical Output Charge and C_{OSS} Stored Energy

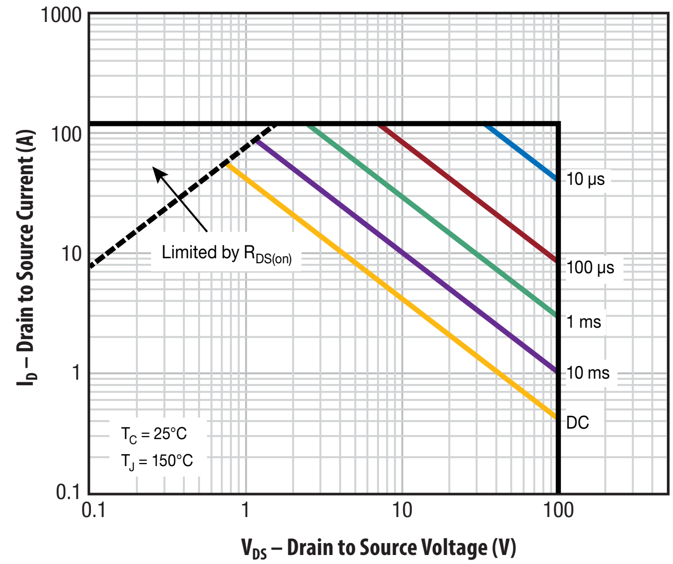


Figure 14. Safe Operating Area

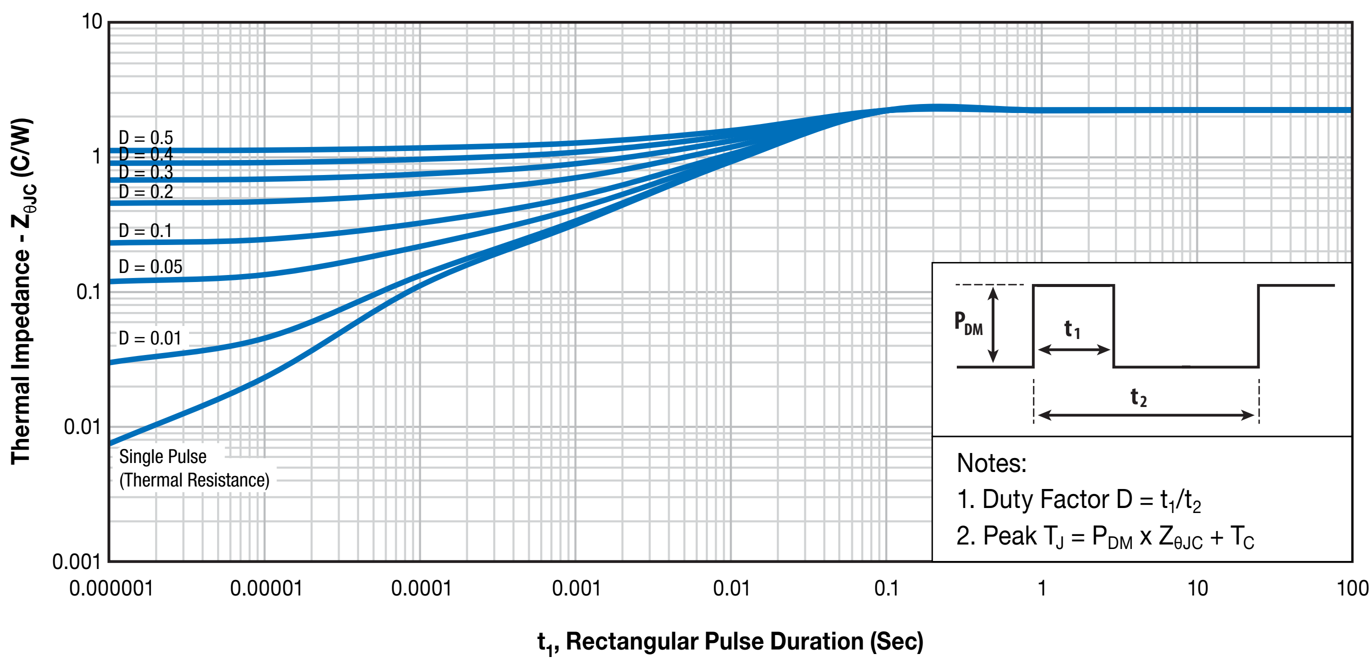
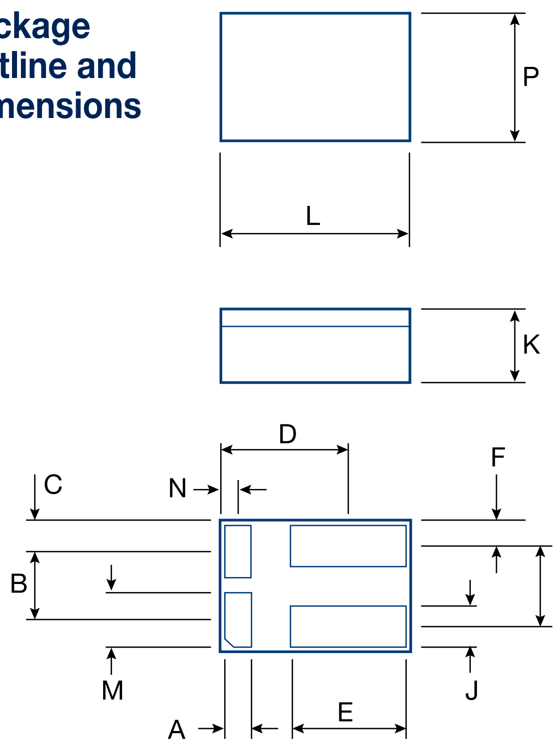


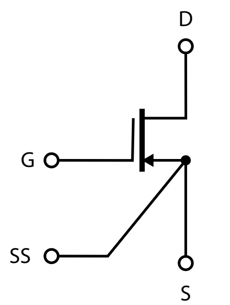
Figure 15. Transient Thermal Impedance, Junction to Case

Package Outline and Dimensions



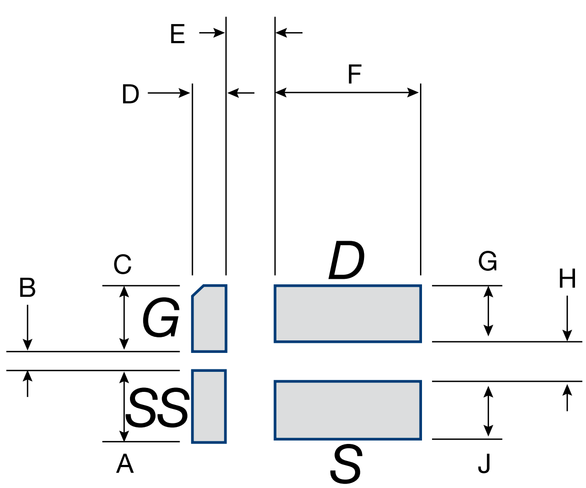
Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
A	0.027	0.037	0.685	0.939	
B	0.073	0.083	1.854	2.108	
C	0.031	0.041	0.784	1.041	
D	0.143	0.153	3.632	3.886	
E	0.129	0.139	3.277	3.531	
F	0.027	0.037	0.686	0.940	
G	0.082	0.092	2.083	2.337	
J	0.050	0.060	1.270	1.524	
K	0.078	0.088	1.981	2.235	Ref. only
L	0.215	0.225	5.461	5.715	
M	0.058	0.068	1.473	1.727	
N	0.016	0.026	0.406	0.660	
P	0.145	0.155	3.683	3.937	

Package Connections



NOTE: SS pin is connected directly to source of internal die.

FSMD-B Footprint for Printed Circuit Board Design



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
A	0.064	0.074	1.626	1.880	
B	0.010	0.020	0.254	0.508	
C	0.064	0.074	1.626	1.880	
D	0.036	0.046	0.914	1.168	
E	0.034	0.044	0.864	1.118	
F	0.135	0.145	3.429	3.683	
G	0.059	0.069	1.499	1.753	
H	0.020	0.030	0.508	0.762	
J	0.059	0.069	1.499	1.753	

Notes

Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.

Note 3. $R_{\theta JA}$ measured with FSMD-B package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 5. Guaranteed by design/device construction. Not tested.

Note 6. Guaranteed by design/device construction. Not tested. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}).. The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time ((I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{Dc}

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