

Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
 - SEE immunity for LET of 83.2 MeV/(mg/cm²) in Si with V_{DS} up to 100% of rated Breakdown
- Neutron
 - Maintains Pre-Rad specification for up to 4×10^{15} Neutrons/cm²



EPC7004BSH

**Rad-Hard eGaN® 100 V, 46 A,
16 mΩ typ Surface Mount (FSMD-B)**

Description

EPC Space FSMD-B series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Applications

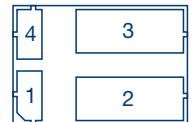
- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	35	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	2.25	

I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	SS	Source Sense



Absolute Maximum Rating ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	100	V
I_D	Continuous Drain Current I_D @ $V_{GS} = 5\text{ V}$, $T_C = 25^\circ\text{C}$	46	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} \leq 80\text{ }\mu\text{s}$	184	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1A (ΔA)	
Weight	Device Weight	0.135	g

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	V_{DSMAX}	$V_G = 0\text{ V}$	100			V
Drain to Source Leakage	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$		0.36	250	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, T_J = 125^\circ\text{C}$		3.1	500	
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 6\text{ V}$		10	600	
Gate to Source Forward Leakage		$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		20	1000	
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4\text{ V}$		0.36	250	
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 8\text{ mA}$	0.8	1.4	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)} / \Delta T$			1.26		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$V_{GS} = 5\text{ V}, I_D = 46\text{ A}$		13	16	m Ω
Source to Drain Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$		1.7	3	V

Dynamic Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		797	1400	pF
Reverse transfer Capacitance	C_{RSS}			1.8	30	
Output Capacitance	C_{OSS}			411	700	
Effective Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		522		
Effective Output Capacitance, Time Related	$C_{OSS(TR)}$			690		
Total Gate Charge (Note 6)	Q_G	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 30\text{ A}$		7	11	nC
Gate to Source Charge (Note 6)	Q_{GS}	$V_{DS} = 50\text{ V}, I_D = 30\text{ A}$		2.4	6	
Gate to Drain Charge (Note 6)	Q_{GD}			1.7	3.5	
Output Charge (Note 5)	Q_{OSS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		35		
Source to Drain Recovery Charge (Note 5)	Q_{RR}	$I_D = 15\text{ A}, V_{DS} = 50\text{ V}$		0		

Radiation Characteristics

Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON	$V_{GS} = 5 \text{ V}$
NO BIAS	$V_{DS} = V_{GS} = 0 \text{ V}$
OFF	$V_{DS} = 80\% B_{V_{DSS}}$

Electrical Characteristics up to 1000 krad ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	$V_{GS} = 0 \text{ V}$	100			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 8 \text{ mA}$	0.8	1.4	2.5	
Drain to Source Leakage	I_{DSS}	$V_{GS} = 0 \text{ V}, V_{DS} = 100 \text{ V}$		0.36	250	μA
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 6 \text{ V}$		10	600	
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4 \text{ V}$		0.36	250	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$I_D = 46 \text{ A}, V_{GS} = 5 \text{ V}$		13	16	$\text{m}\Omega$

Typical Single Event Effect Safe Operating Area

Note : All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.

Test		Environment			V_{DS} Voltage (V)	
See SOA	Ion	LET $\text{MeV}(\text{mg}/\text{cm}^2)$ in Si (+/-5%)	Range μm (+/- 7.5%)	Energy MeV (+/-10%)	$V_{GS} = 0 \text{ V}$	$V_{GS} = -4\text{V}$
	Xe	63.6	71.3	963	100	100
	Au	83.2	121.4	2256	100	100

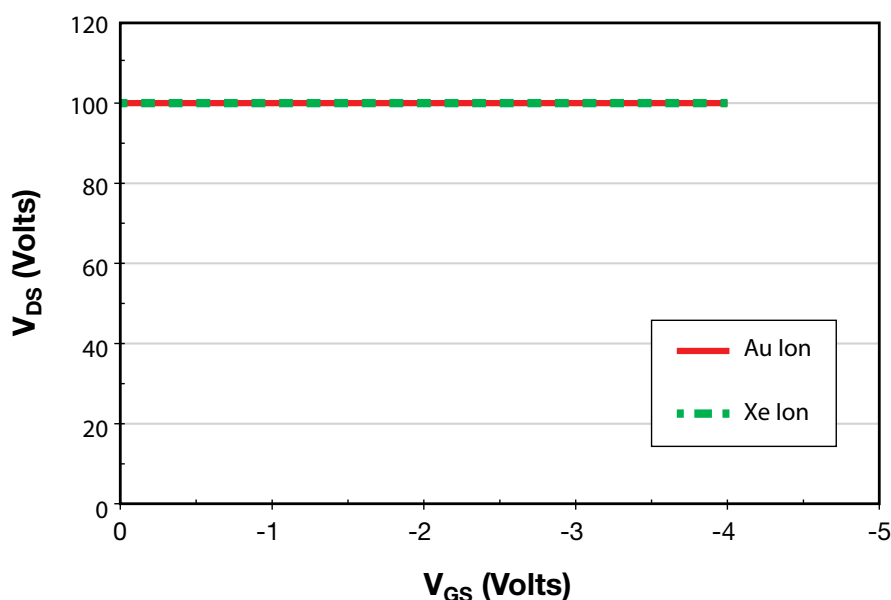


Figure 1. Typical Single Event Effect Safe Operating Area

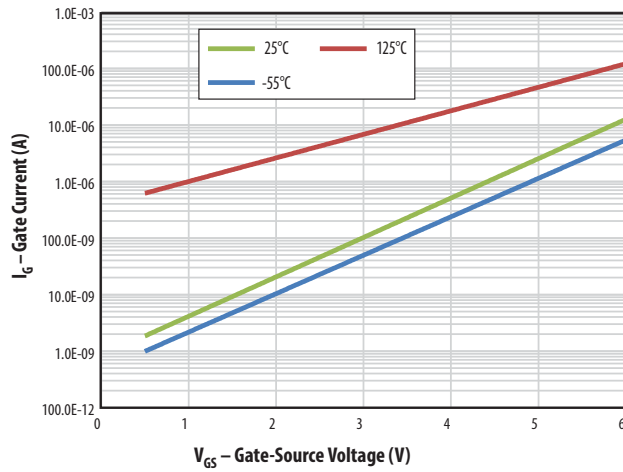


Figure 2. Typical Gate-Source Leakage Current vs. Ambient Temperature

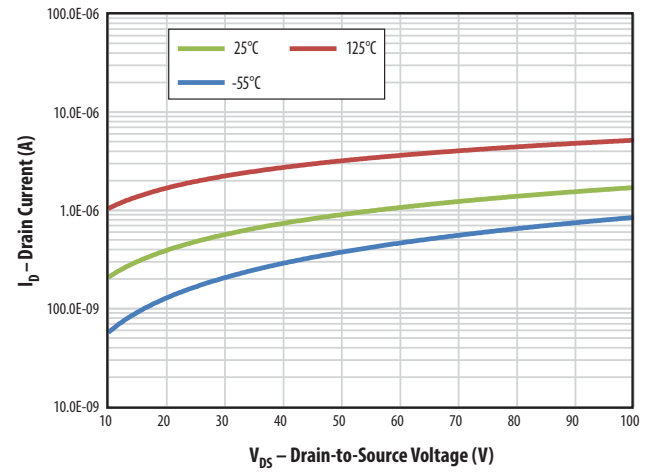


Figure 3. Typical Drain-Source Leakage Current vs. Ambient Temperature

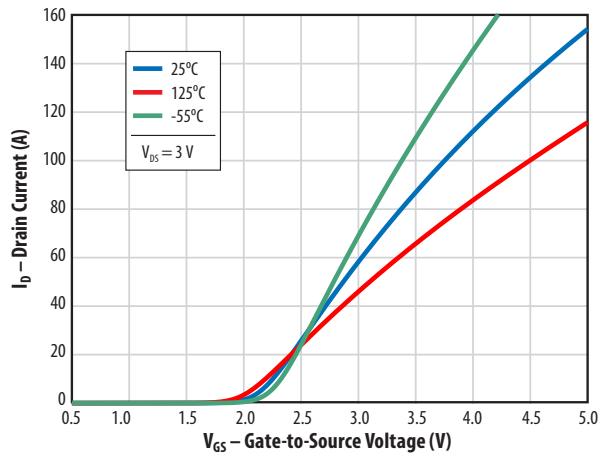


Figure 4. Typical Transfer Characteristics

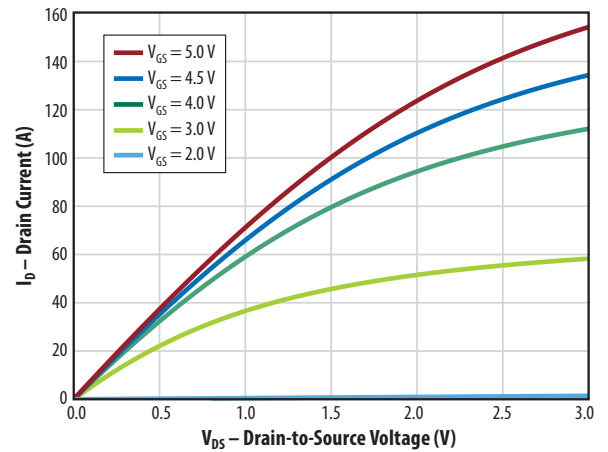


Figure 5. Typical Output Characteristics at 25°C

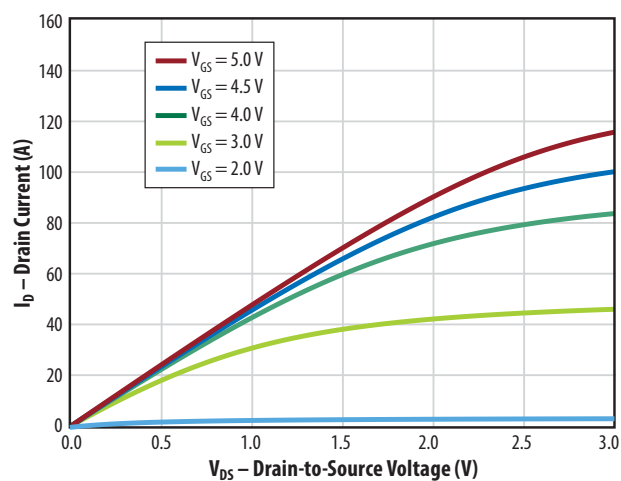


Figure 6. Typical Output Characteristics at 125°C

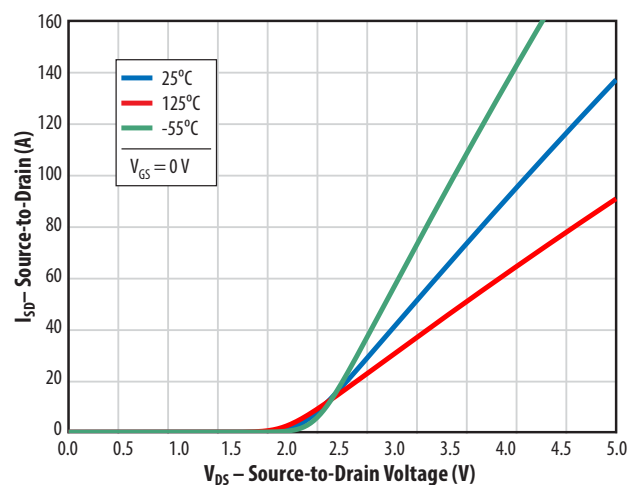
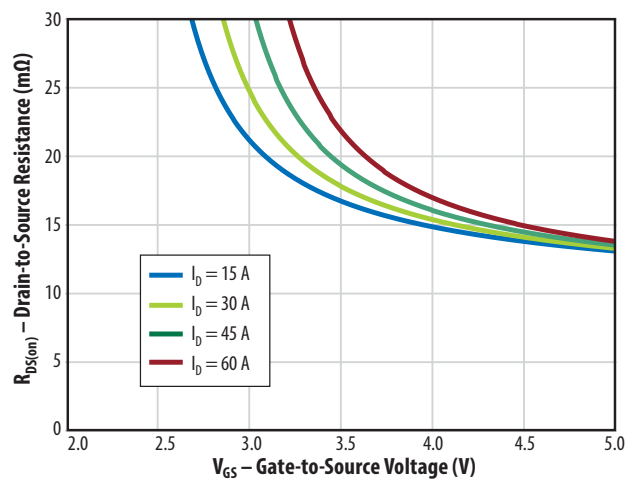
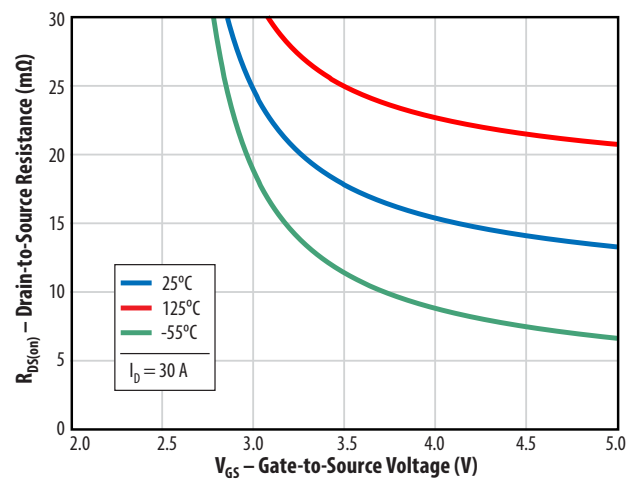


Figure 7. Reverse Drain-Source Characteristics

Figure 8. $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 9. $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

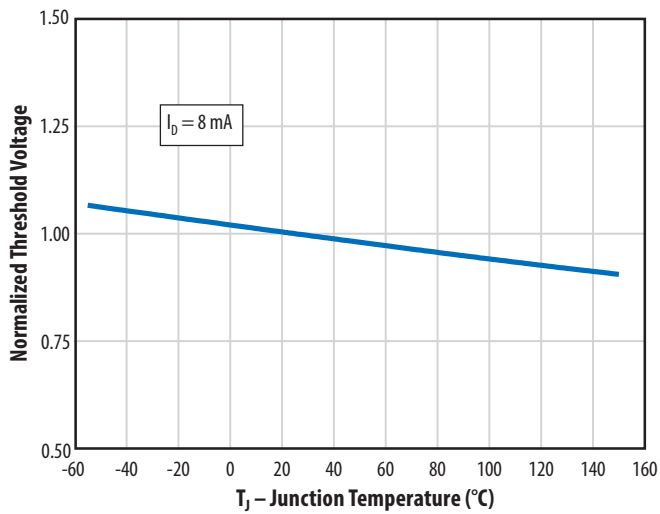


Figure 10. Normalized Threshold Voltage vs. Temperature

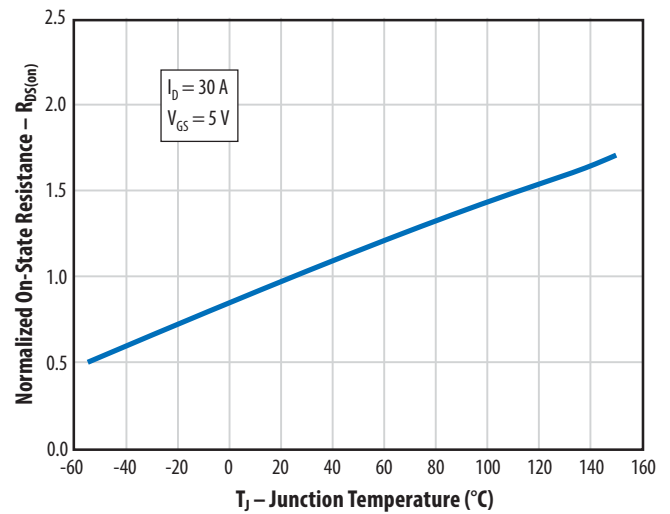


Figure 11. Normalized On-State Resistance vs. Temperature

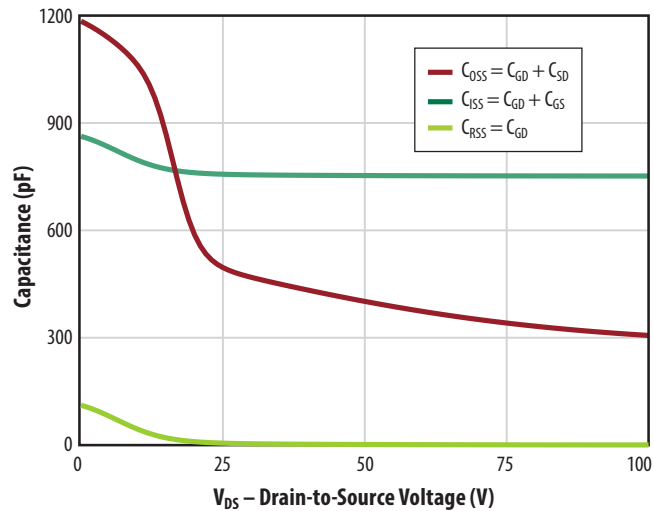


Figure 12. Typical Capacitance

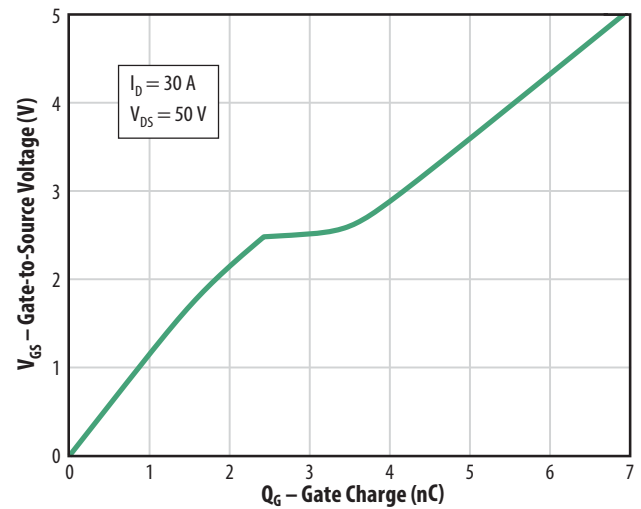


Figure 13. Typical Gate Charge

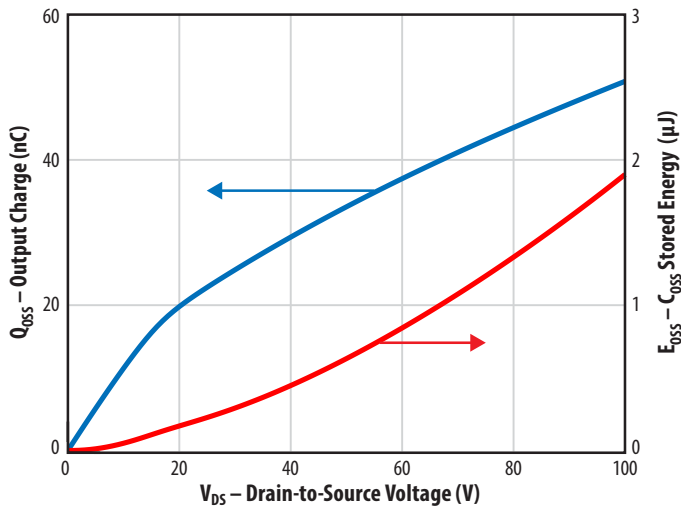


Figure 14. Typical Output Charge and C_{oss} Stored Energy

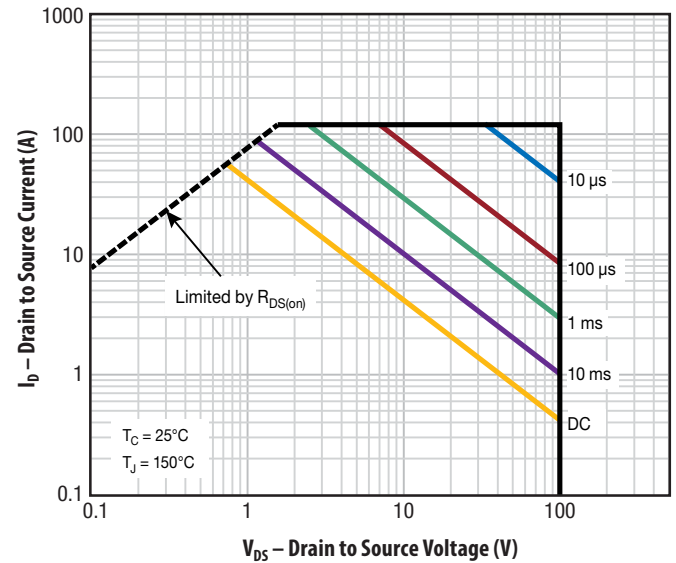


Figure 15. Safe Operating Area

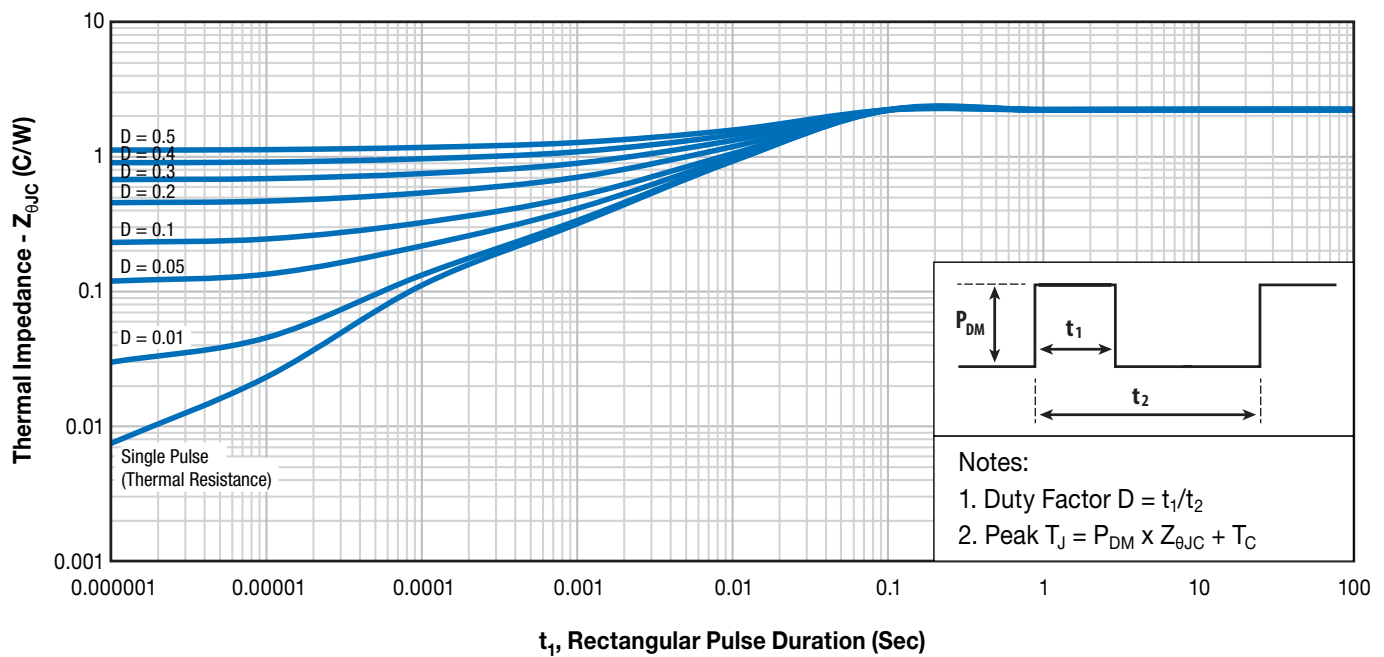
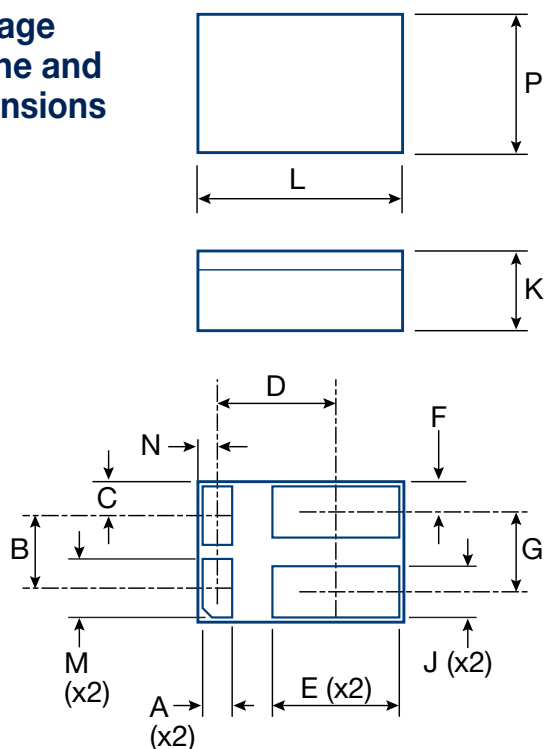


Figure 16. Transient Thermal Impedance, Junction to Case

Package Outline and Dimensions

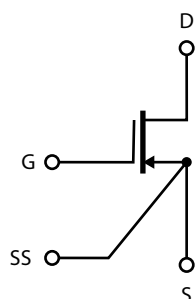


Symbol	IN		MM	
	NOM	REF	NOM	REF
A	0.032		0.81	
B	0.078		1.98	
C		0.036		0.91
D	0.127		3.23	
E	0.137		3.48	
F		0.032		0.81
G	0.087		2.21	
J	0.05		1.27	
K		0.083		2.11
L	0.22		5.59	
M	0.063		1.6	
N		0.021		0.53
P	0.15		3.81	

Note: All dimensions have a tolerance of ± 0.005 in [± 0.13 mm]

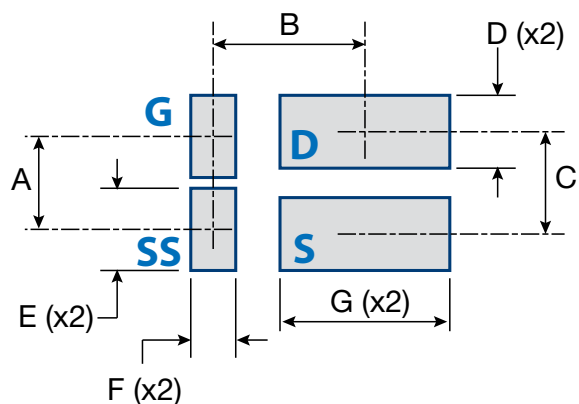
Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb

Package Connections



NOTE: SS pin is connected directly to source of internal die.

FSMD-B Footprint for Printed Circuit Board Design



Symbol	IN	MM	Note
	NOM	NOM	
A	0.078	1.98	
B	0.127	3.23	
C	0.087	2.21	
D	0.061	1.55	
E	0.069	1.75	
F	0.038	0.97	
G	0.142	3.61	

Suggested footprint:

NOM. DIM = .003 in [0.08 mm] swell on average

Notes

- Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.
- Note 3. $R_{\theta JA}$ measured with FSMD-B package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 μ s and duty cycle is 1%, maximum.
- Note 5. Guaranteed by design/device construction. Not tested.
- Note 6. Guaranteed by design/device construction. Not tested. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S . The gate current is adjusted to yield the desired charge per unit time ($(I_{const} \cdot \text{time per division})$) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch t_{off}/t_{on} should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC} .

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