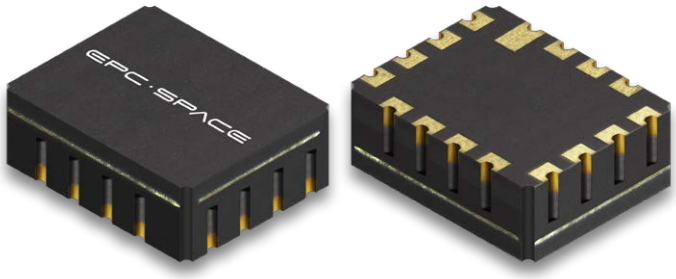
Features

- Compatible with all EPC Space Discrete eGaN® products
- Single GAN Gate Driver Integrated Circuit
- Independent Pull-Up and Pull-Down gate drive outputs
- Capable of Driving 5000 pF+ Loads
- High Speed Capability: 3.0 MHz+
- 3 V Logic-Compatible Input control
- Non-Inverting and Inverting Logic Inputs
- 8 V–14 V Supply for Interface to Distributed Bias Systems
- Hermetic Ceramic QLCC SMT Package
- Extremely Small Size: 5.8 x 4.6 x 2.2 mm

Applications

- DC-DC conversion
- Satellite Electrical
- Power Switches/Actuators
- Motor Drivers



EPC7009L16C

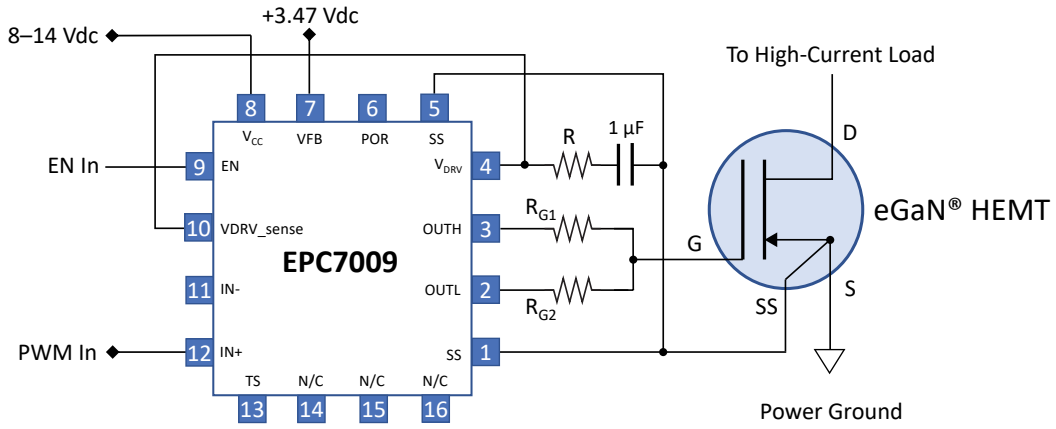
Radiation-Hardened Single Output GaN Gate Driver Monolithic IC

Description

The EPC7009L16C is a radiation hardened, high-speed gate-driver, implemented as an integrated circuit (IC) using EPC's proprietary eGaN® technology. The EPC7009 GaN IC contains an on-chip 8 V–14 V to 5 V linear regulator, under-voltage lockout protection and independent pull-up and pull-down outputs to both optimize and simplify the gate-drive to an external GaN FET. The IC is packaged in an innovative, space-saving hermetic 16-pin SMT package.

Typical Application Circuit

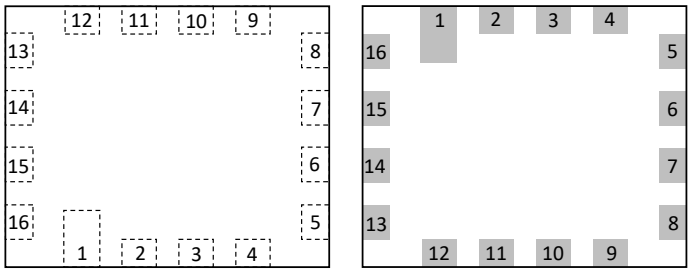
Non-Inverting Mode Low-Side eGaN® HEMT Gate Driver



EPC7009L16C Pinout

16 Pin QLCC SMT Package

Top (X-Ray) View **Bottom (Pad) View**



EPC7009L16C Pin Descriptions and Functionality

Pin #	Pin Name	(I)nput, (O)utput, (P)ower	Pin Function
1	SS	P	Gate driver ground return that is connected to the “Source Sense” (SS) pad on EPC Space eGaN HEMTs. Keep the connection from the SS pin to the Source pad as short as possible. The substrate of the IC is also connected to the SS pin.
2	OUTL	O	Gate driver high peak current pull-down output. When ON, the OUTL output is pulled down to the SS potential. In most applications this pin should be connected directly to the gate pad of EPC Space eGaN HEMTs. Keep the connection from the OUTL pin to the Gate pad as short as possible.
3	OUTH	O	Gate driver high peak current pull-up output. When ON, this output is pulled up to the VDRV potential. A low value resistor (10 W, maximum) may be connected in series with the OUTH pin and the Gate pad of EPC Space eGaN HEMTs in order to slow down the rise time of the HEMT being driven. Keep the connection from the OUTH pin (and through the optional gate resistor) to the Gate pad as short as possible.
4	VDRV	P	Regulated 5.0 V supply voltage. Connect a 1Ω resistance and 1.0 µF, minimum, bypass capacitor from VDRV to SS.
5	SS	P	Gate driver ground return that is connected to the “Source” pad on EPC Space eGaN HEMTs. Keep the connection from the SS pin to the Source pad as short as possible. The substrate of the IC is also connected to the SS pin.
6	POR	O	Power-On-Reset output. IC is NOT active when POR is logic 0. External pull-up resistor to be connected between VCC and POR
7	VFB	I	Adjustable reference input voltage for linear regulator.
8	VCC	P	External 10 V power supply connection referenced to SS.
9	EN	I	Internal linear regulator enable input (low OFF, high ON)
10	VDRV_sense	I	Sense node input for voltage linear regulator
11	IN-	I	Negative logic input, level referenced to SS. Output will be high when IN- < VIL with IN+ = VDRV. This input has an internal pull-down resistor to SS.
12	IN+	I	Positive logic input, level referenced to SS. Output will be high when IN+ > VIH with IN- = SS or floating. This input has an internal pull-down resistor to SS.
13	TS	--	Temperature Sense input referenced to SS. Resistance varies with temperature.
14	NC	--	No connection
15	NC	--	No connection
16	NC	--	No connection

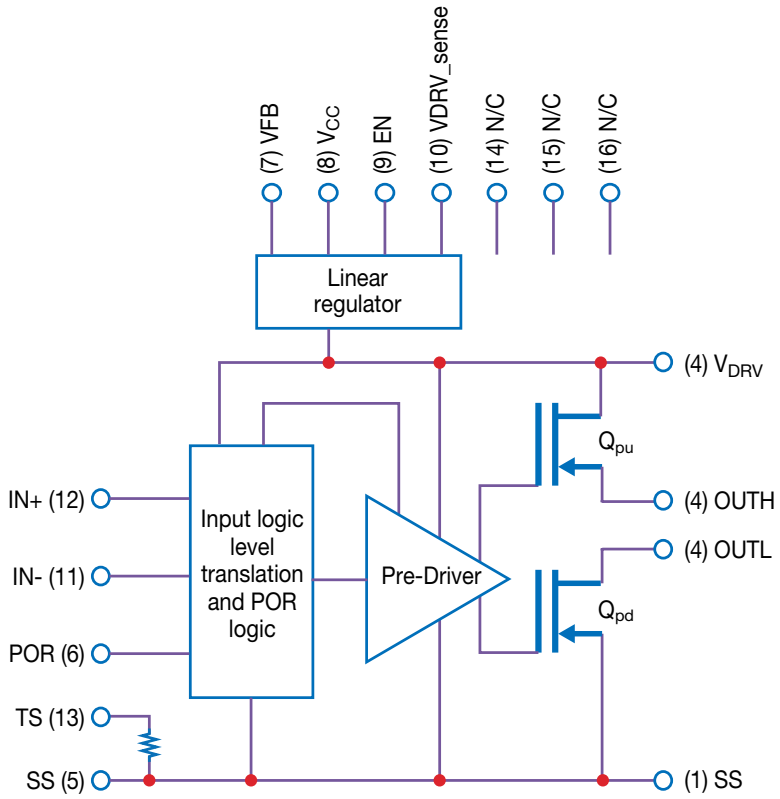


Figure 1. EPC7009 Simplified Functional Block Diagram

Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Min	Max	Units
V_{CC}	Input Supply Voltage		14	V
V_{DRV}	Regulated Gate Driver Voltage		6	
IN+, IN-, EN, POR	Logic Input Voltage Range	-1	5.5	
VFB	Regulator Feedback Adjustment Voltage Range	-1	5.5	
TS	Temperature Sensor Resistor Input Voltage Range	-1	5.5	
T_{STG}	Storage Junction Temperature Range	-55	+150	°C
T_J	Operating Junction Temperature Range	-55	+125	
T_C	Case Operating Temperature Range	-55	+110	
T_{sol}	Package Mounting Surface Temperature		230	
ESD	ESD Class Level (HBM)		1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Case-to-Ambient (Note 3)	TBD	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case (Note 3)	TBD	

Recommended Operating Conditions *(T_C = -55 to 125°C unless otherwise noted) All voltages referenced to SS*

Symbol	Parameter-Conditions	MIN	TYP	MAX	Units
V_{CC}	Input Supply Voltage	8	12	13	V
V_{DRV}	Regulated Gate Driver Voltage	4.5	5	5.5	
IN+, IN-	Logic Input Voltage Range	0		5	
EN, POR	Other Input Voltage Range	0		5	
VFB	Regulator Feedback Adjustment Voltage Range (Note 7)	3.10		3.8	
TS	Temperature Sensor Resistor Input Voltage Range	0		5	

OUTPUT Static Electrical *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
V_{OL}	OUTL Low-Level Voltage	V_{DRV} = 5 V_{DC}, IN+ = 0.8 V_{DC}, I_{OUTL} = 100 mA (Note 1)	T_C = 25°C		0.015		V
			T_C = -55°C T_C = 110°C				
V_{OH}	OUTH High-Level Voltage	V_{DRV} = 5 V_{DC}, IN+ = 3 V_{DC}, I_{OUTH} = -100 mA (Note 1)	T_C = 25°C		4.98		
			T_C = -55°C T_C = 110°C				
$R_{DS(on)}$	OUTL Pull-Down ON-State Resistance (OUT_L -SS)	V_{DRV} = 5 V_{DC}, IN+ = 0.8 V_{DC}, I_{OUT} = 0.25 A (Notes 1, 2)	T_C = 25°C		0.14		Ω
			T_C = -55°C T_C = 110°C				
$R_{DS(on)}$	OUTH Pull-Up ON-State Resistance (V_{DRV} -OUT_H)	V_{DRV} = 5 V_{DC}, IN+ = 3 V_{DC}, I_{OUT} = -0.25 A (Note 1, 2)	T_C = 25°C		0.18		
			T_C = -55°C T_C = 110°C				

INPUT Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{IL}	Low Logic Level Input Voltage	V_{DRV} = 5 V_{DC}, IN+/IN- Falling (Note 4)			0.8	V
V_{IH}	High Logic Level Input Voltage	V_{DRV} = 5 V_{DC}, IN+/IN- Rising (Note 5)	2.4			
V_{HYST}	Input Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		0.3		
R_{IL_IN-}	Logic Input Pull-Down Resistance	(Note 6)		8		kΩ
R_{IL_IN+}				8		
R_{EN}	Enable Pull-Down Resistance	EN = 5V		50		
R_{VFB}	VFB Pull-Down Resistance	VFB = 3.47V		50		

V_{CC}, V_{FB} and V_{DRV} Static Electrical Characteristics *(-55°C ≤ T_C ≤ 110°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
V_{CC}	V_{CC} Operating Voltage Range		8	12	14	V
$I_{CC0\ (sleep)}$	V_{CC} Sleep Mode Quiescent Current	IN+ = 0 V_{DC}, IN- = 0 V_{DC}, EN = 5 V_{DC}		2.5		mA
$I_{CCQ\ (run)}$	V_{CC} Run Mode Quiescent Current	IN+ = 0 V_{DC}, IN- = 5 V, EN = 0 V		9		
$I_{CC(250k)}$	V_{CC} Total Operating Current: 250 kHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		10		
$I_{CC(1M)}$	V_{CC} Total Operating Current: 1 MHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		20		
V_{DRV}	Regulated Gate Driver Voltage	V_{DRV} to SS (Note 7)	4.9	5	5.1	V
V_{CC} to V_{DRV}			3			
I_{DRVQ}	V_{DRV} Off State Quiescent Current	IN+ = 0 V_{DC}, IN- = 0 V_{DC}, EN = 0 V_{DC}		7		mA
I_{DRV_250kHz}	V_{DRV} Operating Current: 250 kHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		9		
I_{DRV_1MHz}	V_{DRV} Operating Current: 1 MHz	V_{DRV} = 5 V_{DC}, IN+ = 0-5V, f_s = 250 kHz, 50% On-Time		19		

Under-Voltage Lockout Static Electrical Characteristics *(-55°C ≤ T_C ≤ 125°C unless otherwise noted)*

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
UVLO+	V_{DRV} UVLO Rising Threshold		2.5	2.9	3.8	V
UVLO–	V_{DRV} UVLO Falling Threshold		2.2	2.6	3.5	
UVLO+ UVLO–	V_{DRV} UVLO Hysteresis to Falling Threshold			0.3		
R_{POR}	POR pull-down open drain FET $R_{DS(on)}$	POR = 0.5 V		22		Ω

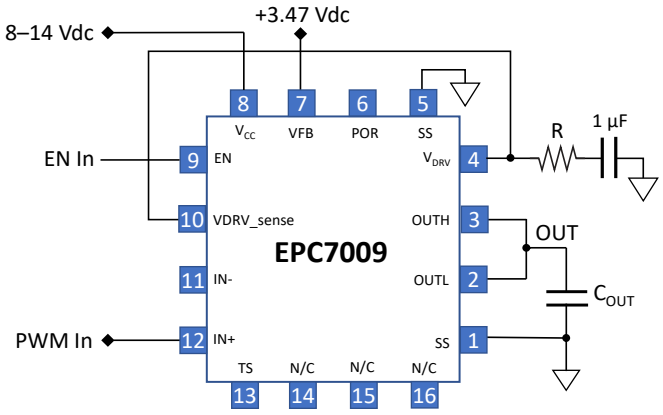
Power Driver Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
$t_{d(on)}$	IN+/IN- -to-OUT Turn-ON Delay Time	V_{DRV} = 5 V_{DC}; C_{OUT} = 2200 pF (See Figures 2, 3, 4 and 5)			35		ns
$t_{d(off)}$	IN+/IN- -to-OUT Turn-OFF Delay Time				35		
t_r	OUT Rise Time	V_{DRV} = 5 V_{DC} (See Figures 2, 3, 4 and 5)	C_{OUT} = 1000 pF		1.6		
			C_{OUT} = 2200 pF		2.2		
			C_{OUT} = 5100 pF		4		
t_f	OUT Fall Time		C_{OUT} = 1000 pF		1.2		
			C_{OUT} = 2200 pF		2		
			C_{OUT} = 5100 pF		4		

Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

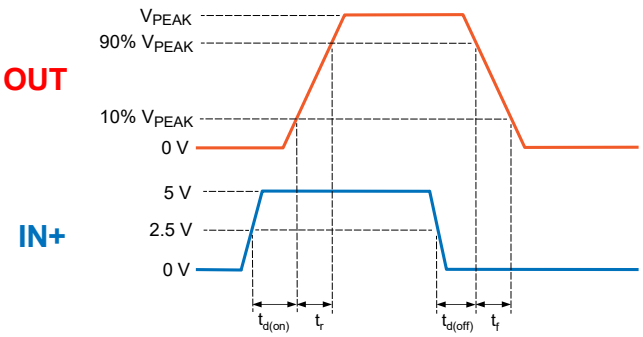
Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
PW	Minimum Pulse Width, ON or OFF	V_{DRV} = 5 V_{DC}	50			ns

Switching Figures



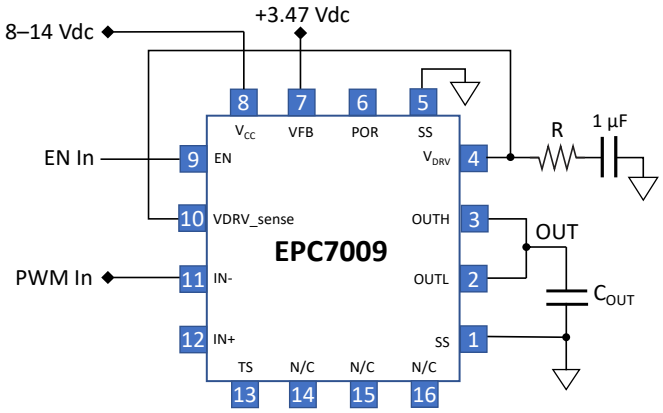
Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 2. IN+ -to-OUT Switching Time Test Circuit



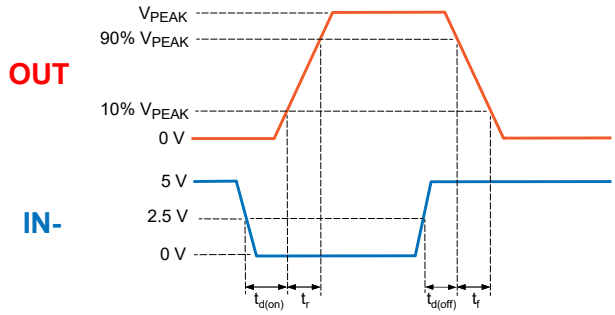
NOTE: Waveforms exaggerated for clarity and observability.

Figure 3. IN+ -to-OUT Switching Time Definition



Only pins connected during testing identified.
Pulse Generator set to 500 kHz frequency, 5% duty cycle.

Figure 4. IN- -to-OUT Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 5. IN- -to-OUT Switching Time Definition

Specification Notes

1.) V_{DRV} = +5 V_{DC}, SS = 0 V_{DC}.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When the logic input (IN+) is at the low input voltage level the OUTL output is guaranteed to be ON (~SS potential) and the OUTH output is guaranteed to be OFF (open).

5.) When the logic input (IN+) is at the high input voltage level the OUTH output is guaranteed to be ON (~V_{DRV} potential) and the OUTL output is guaranteed to be OFF (open).

6.) Pull-down to SS for IN+ and V_{DRV} for IN-.

7.) The regulated output voltage, V_{DRV}, is 1.44 x V_{FB}, nominal. For a nominal 5 V_{DC} output for V_{DRV}, V_{FB} = 3.47 V_{DC}. The gate driver potential V_{DRV} may be adjusted to any value within the V_{FB} specified range.

EPC7009 Operational Truth Table

The truth table for the logic inputs and the power supply UVLO circuit is shown in the following table. In the following table, OUT is the combined driver output when OUTL and OUTH are connected together.

All conditions in the table are valid when V_{BIAS} and V_{DRV} are greater than UVLO+. When V_{CC} and V_{DRV} are less than ULVO+ rising or UVLO+ falling, OUT is in the low (L) state, approximately the SS potential, regardless of the state of either logic input.

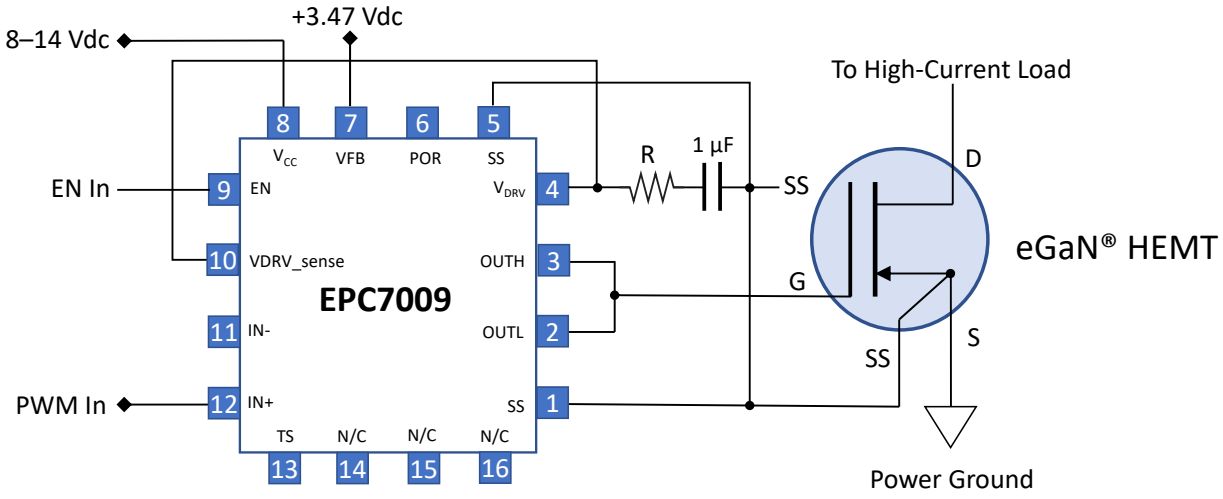
VDRV	EN	POR	IN+	IN-	OUT *	OUT H	OUT L
<UVLO	-	0	-	-	L	Hi-Z	0
0**	0	-	-	-	L	Hi-Z	0
>UVLO	1	1	0	0	L	Hi-Z	0
	1	1	1	0	H	1	Hi-Z
	1	1	0	1	L	Hi-Z	0
	1	1	1	1	L	Hi-Z	0

**OUT is the combined driver output when OUTL and OUTH are connected together*
***after the complete discharge of the external capacitor*

Application Information

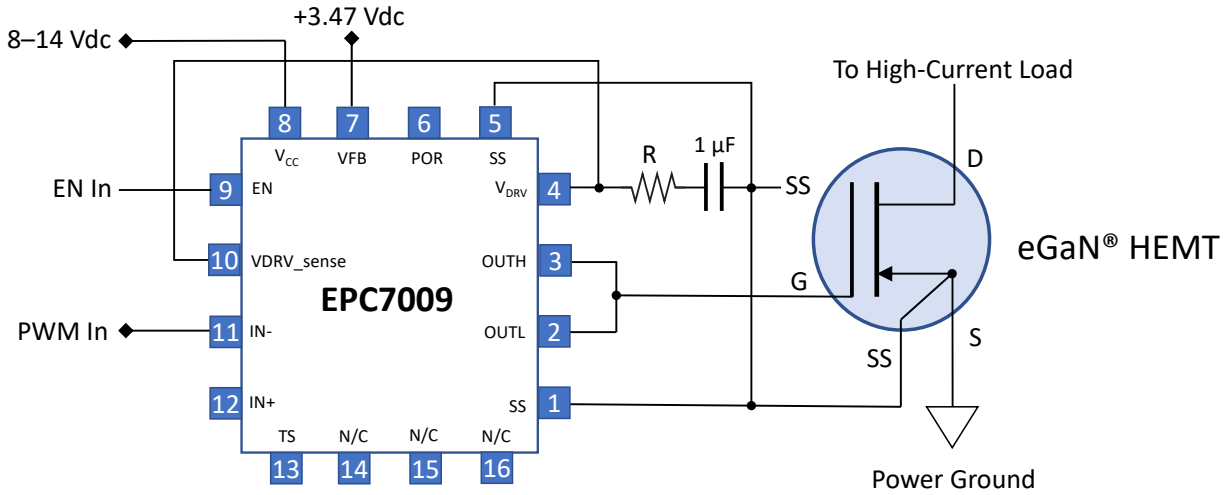
The following figures detail the suggested applications for the EPC7009 integrated circuit. For all applications, please refer to the following sections for proper power supply bypassing and layout recommendations and criteria.

In all the following figures, only the pins that are considered or that require connection are identified.



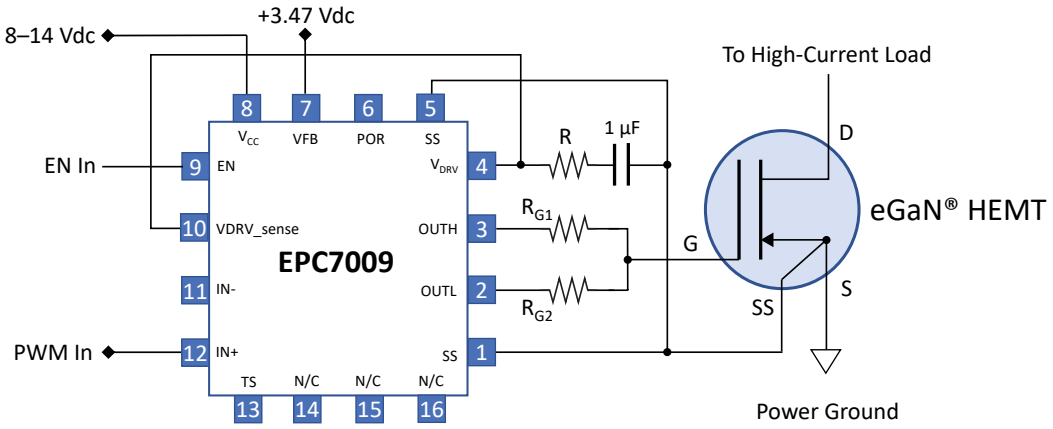
Note: Keep Out-to-Gate and SS-to-Source-Sense connections as short as possible.

Figure 7. Non-Inverting Mode Low-Side Driver and EPC Space eGaN® HEMT



Note: Keep Out-to-Gate and SS-to-Source-Sense connections as short as possible.

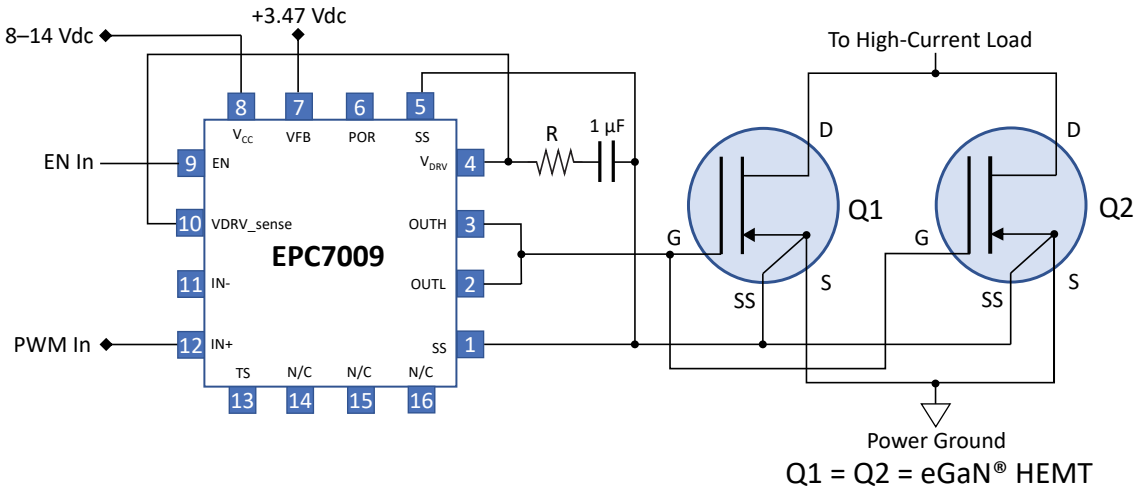
Figure 8. Inverting Mode Low-Side Driver and EPC Space eGaN® HEMT



Note: Make all OUTH-to-RG1, OUTL-to-RG2, the tie point of RG1/RG2-to-Gate and SS-to-Source Sense connections of equal length and as short as possible. RG1/RG2 are 20 Ω, maximum

Figure 9. Non-Inverting Mode Low-Side Driver and EPC Space eGaN® HEMT with Gate Damping/Slow-Down Resistors

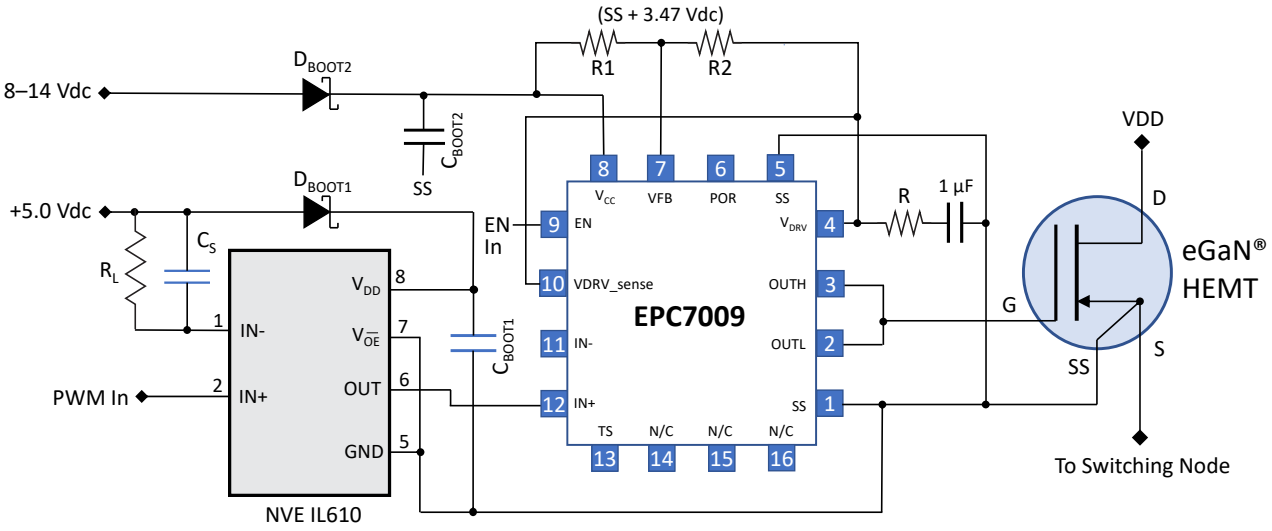
In Figure 9 resistor RG1 is used to control the rise time of the eGaN® HEMT and resistor RG2 is used to control the fall time. Such resistors are often utilized to reduce EMI or to minimize voltage overshoot and ringing on the V_{DD} bus local to the high current being switched by the eGaN HEMT.



Note: Make all OUTH/OUTL-to-Gate, SS-to-Source Sense and Source connections as short as possible. Also keep the Drain connections as short as physically possible.

Figure 10. Non-Inverting Mode Low-Side Driver Driving Multiple, Parallel EPC Space eGaN® HEMTs

For parallel the parallel HEMT configuration as shown in Figure 10, the number of HEMT devices that may be driven in parallel is determined by the C_{ISS} of the individual HEMTs and the capacitive drive capability of the EPC7009 gate driver integrated circuit.



Note: Make all OUTH/OUTL-to-Gate, SS-to-Source Sense and Source connections as short as possible. Also keep the Drain connections as short as physically possible. The SS node may be treated as a local etch plane in the area of the IL610, the EPC7009 and the eGaN® HEMT. Circuit shown utilizes dual bootstrapping: one for the NVE IL610 and one for the EPC7009.

Figure 11. Non-Inverting Mode Low-Side Driver Driving Multiple, Parallel EPC Space eGaN® HEMTs

Package Outline Dimensions

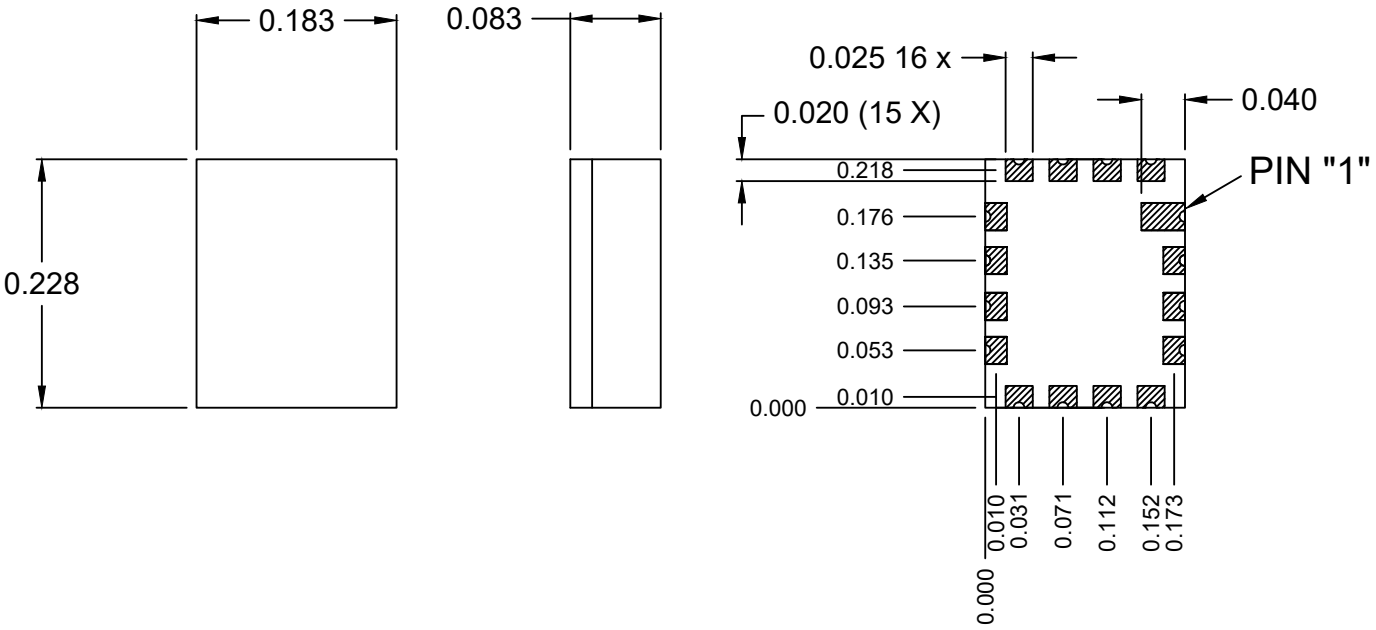


Figure 12. EPC7009L16C Package Outline Dimensions

Recommended PCB Solder Pad Configuration

To prevent damage to the internal circuitry it is important that the EPC7009L16C integrated circuit be soldered to the PCB motherboard using SN63 (or equivalent) solder. The recommended PCB pad dimensions and locations are shown in Figure 13.

All dimensions are shown in inches.

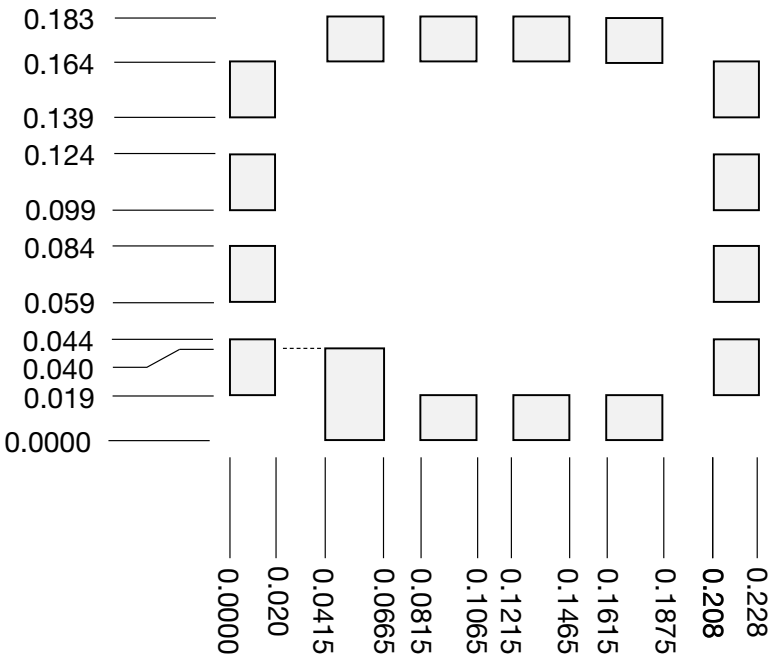


Figure 13. Recommended PCB Solder Pad Configuration (Top View)

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