## Features

- 80 $V_{DC}$ / 6 A Half-Bridge Driver
- 14 mΩ (typ), integrated high side and low-side eGaN FETs
- Integrated GaN gate driver and level-shifter
- 12 V external bias supply
- 3.3 V or 5 V input logic levels
- Independent high side and low side control inputs
- Logic Input Shoot-Through Protection, commands both FETs off when control inputs are both high at the same time
- Internal Under-Voltage Lockout (UVLO) Circuitry
- Synchronous charging for high side bootstrap supply
- Flexible power-sequencing with active gate pull-down for HS and LS FET allows for $V_{IN}$ before $V_{BIAS}$ power-up
- High Speed Switching Capability: 2+ MHz
- Compact AlN Ceramic SMT Package (L7)
- Total Ionizing Dose:
  - Rated to 300 kRad
- Single Event:
  - SEE immunity for LET of 61 MeV/mg/cm$^2$ with $V_{DD}$ up to 100% of Rated Voltage
- Neutron Fluence:
  - Maintains specification up to 1 x 10$^{15}$ N/cm$^2$

# EPC7012L7BH

**80 $V_{DC}$ / 6 A Radiation-Hardened GaN Power Stage**

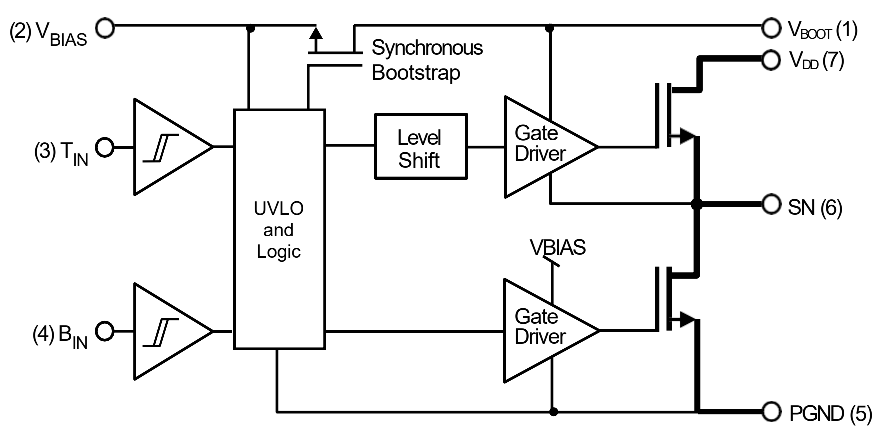
## Description

The EPC Space EPC7012L7BH, is a radiation-hardened, half-bridge GaN power stage. Input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with eGaN output FETs, configured as a half-bridge, integrated within a monolithic chip in a custom 7-pin Aluminum Nitride SMT ceramic package. Datasheet parameters are “Post Radiation Effects”. 80 $V_{DC}$ maximum operating voltage, 100V rated internal power transistors.

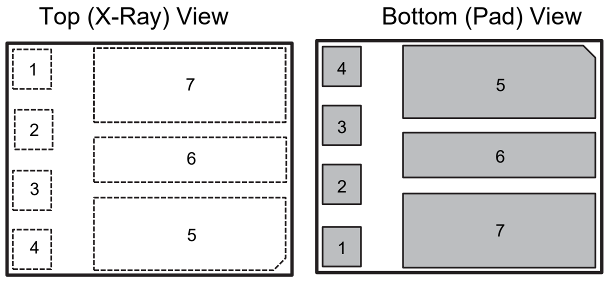
## Applications

- Single and Multi-Phase Motor Drivers:
  - Reaction Wheel Assemblies (RWAs)
  - Momentum Wheels
  - Robotic Actuators
- Half-Bridge/POL Power Supplies:
  - Low Current Single Phase
  - High Current Multi-Phase
- Satellite Electrical Power System

## EPC7012L7BH Functional Block Diagram



**7-Pin AIN Ceramic SMT Package**




### EPC7012L7BH Configuration and Pin Assignment Table

| Pin # | Pin Name | Type | Pin Function |
|---|---|---|---|
| **1** | $V_{BOOT}$ | P/I | High-Side Driver Floating Power Supply |
| **2** | $V_{BIAS}$ | P/I | +12$V_{DC}$, Nominal, Gate Driver Power Supply Bias Voltage |
| **3** | $T_{IN}$ | L/I | High-Side Switch Logic Input |
| **4** | $B_{IN}$ | L/I | Low-Side Switch Logic Input |
| **5** | PGND | H | Power and Logic Supply Return (High Current) |
| **6** | SN | P/O/H | Switching Node (High dV/dt, High Current) |
| **7** | $V_{DD}$ | P/I/H | Positive Power Supply Input (High Current) |

KEY: P = Power, L= Logic, I= Input, O = Output, H = High Current Connection, GR = Ground Return

## Pin Descriptions

**$V_{BOOT}$ (Pin 1)**
High-Side Driver Floating Power Supply. The floating bootstrap high-side driver power supply referenced to the SN output (pin 6). For proper operation, connect an external bootstrap capacitor (0.1 μF recommended) from $V_{BOOT}$ to SN.

**$V_{BIAS}$ (Pin 2)**
The raw DC bias power supply referenced to GND that supplies power to the low-and high-side gate drivers and to the internal logic in the EPC7012L7BH. Connect two external bypass capacitors (0.1 μF and 10 μF recommended) from $V_{BOOT}$ to PGND (Pin 7).

**$T_{IN}$ (Pin 3)**
The $T_{IN}$ pin is the logic input for high-side power driver. When the $T_{IN}$ input pin is logic low (“0”), the high-side output ($V_{DD}$-SN) pins (pins 5 and 6) are in the OFF (high impedance) state. When the $T_{IN}$ input pin is logic high (“1”), the $V_{DD}$-SN pins are in the ON (low impedance) state.

**$B_{IN}$ (Pin 4)**
The $B_{IN}$ pin is the logic input for low-side power driver. When the $B_{IN}$ input pin is logic low (“0”), the low-side output (SN-PGND) pins (pins 6 and 7) are in the OFF (high impedance) state. When the $B_{IN}$ input pin is logic high (“1”), the SN-PGND pins are in the ON (low impedance) state.

**PGND (Power Ground) (Pin 5)**
The PGND pin (pin 5) is the ground return connection for the internal power output circuitry and high-speed gate driver circuitry associated with low-side power driver and for the power good and interface logic for the high-side driver. This pin should be connected directly to the system power return/ground plane to minimize common source inductance, and the voltage transients associated with this inductance. This is a high-current connection.

**SN (Switching Node) (Pin 6)**
The SN pin (pin 6) is the high-current power output for the half-bridge driver. This output alternates from high impedance (the low- and high-side power switches OFF when both logic inputs are “0” or “1” simultaneously) to low impedance from the SN pin to PGND (when BIN is logic “1”) to low impedance from the $V_{DD}$ pin (pin 5) to SN (when $T_{IN}$ is logic “1”). This is a high- current connection.

**$V_{DD}$ (Pin 7)**
The $V_{DD}$ pin (pin 7) is the half-bridge power stage input. This pin should be connected directly to the system power ($V_{DD}$) bus via a low impedance connection, preferably through a low impedance power plane. This pin should be properly bypassed to the system power ground (PGND, pin 5) using the guidelines found in the “Recommended $V_{DD}$-to-PGND Power Supply Bypassing” section, following. This is a high-current connection.

## Absolute Maximum Rating *(-55°C ≤ $T_C$ 125°C unless otherwise noted)*

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $V_{DD}$ | Positive Power Supply Input Voltage (Note 1) | 80 | V |
| $I_{DD}$ | Continuous Operating Current | 6 | A |
| $V_{BIAS}$ | Continuous Gate Driver Bias Supply Voltage | 14.0 | V |
| $V_{BOOT}$ | Continuous Bootstrap Supply Voltage | 14.0 | V |
| $B_{IN}$, $T_{IN}$ | $B_{IN}$ or $T_{IN}$ Logic Input Voltage | -0.3 to 5.5 | V |
| $T_{STG}$ | Storage Junction Temperature Range | -55 to +150 | °C |
| $T_J$ | Operating Junction Temperature Range | -40 to +125 | °C |
| $T_C$ | Case Operating Temperature Range | -55 to +125 | °C |
| $T_{sol}$ | Package Mounting Surface Temperature | 230 | °C |
| ESD | ESD class level (HBM) | 1B | |
| | Device Weight | 0.226 | g |

## Thermal Characteristics

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient | 55 | °C/W |
| $R_{\theta JLid}$ | Thermal Resistance Junction to Case: Lid/Top | 5.1 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case: Bottom of the Power Pads | 2.5 | °C/W |

## OUT Power Switch Static Electrical Characteristics *($T_C$ = 25°C unless otherwise noted)*

| Symbol | Parameter | Test Conditions | | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| $I_{DSS}$ | Drain – Source Leakage Current ($V_{DD}$-to-SN or SN-to-PGND) (Note 2) | $V_{DS}$ = 40 $V_{DC}$, $B_{IN}$ = $T_{IN}$ = 0.5 $V_{DC}$ | $T_C$ = 25°C | - | 2 | 200 | µA |
| | | | $T_C$ = 125°C | - | 8 | 200 | |
| | | $V_{DS}$ = 80 $V_{DC}$, $B_{IN}$ = $T_{IN}$ = 0.5 $V_{DC}$ | $T_C$ = 25°C | - | 3 | 200 | |
| | | | $T_C$ = 125°C | - | 9 | 200 | |
| $R_{DS(on)}$ | Drain – Source ON-State Resistance ($V_{DD}$-to-SN or SN-to-PGND) (Notes 3, 4, 5) | $I_D$ = 3 A, $B_{IN}$ = 2.4 $V_{DC}$ or $T_{IN}$ = 2.4 $V_{DC}$ | $T_C$ = 25°C | - | 14 | 22 | mΩ |
| | | | $T_C$ = 125°C | - | 20 | 40 | |
| | | | $T_C$ = -55°C | - | 9 | 16 | |
| | | $I_D$ = 6 A, $B_{IN}$ = 2.4 $V_{DC}$ or $T_{IN}$ = 2.4 $V_{DC}$ | $T_C$ = 25°C | - | 14 | 22 | |
| | | | $T_C$ = 125°C | - | 20 | 40 | |
| | | | $T_C$ = -55°C | - | 9 | 16 | |
| $V_{SD}$ | Source – Drain Clamping Voltage (SN-to-$V_{DD}$ or PGND-to-SN) (Note 5, 6, 7) | $I_D$ = -3 A, $B_{IN}$ = $T_{IN}$ = 0.5 $V_{DC}$ | $T_C$ = 25°C | - | 2.4 | 3 | V |
| | | | $T_C$ = 125°C | - | 2.4 | 4 | |
| | | | $T_C$ = -55°C | - | 2.4 | 3 | |
| | | $I_D$ = -6 A, $B_{IN}$ = $T_{IN}$ = 0.5 $V_{DC}$ | $T_C$ = 25°C | - | 2.4 | 3 | |
| | | | $T_C$ = 125°C | - | 2.4 | 4 | |
| | | | $T_C$ = -55°C | - | 2.4 | 3 | |

### Recommended Operating Conditions *(-55°C ≤ $T_C$ ≤ 125°C unless otherwise noted)*

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $V_{DD}$ | Positive Power Supply Input Voltage (Note 1) | 80 | V |
| $I_{DD}$ | Continuous Operating Current | 6 | A |
| $V_{BIAS}$ | Continuous Bias Supply Voltage | 11 - 13 | V |
| $V_{BOOT}$ | Continuous Bootstrap Supply Voltage | 11 - 13 | V |

### $B_{IN}$, $T_{IN}$ Logic Input Static Electrical Characteristics *(-55°C ≤ $T_C$ ≤ 125°C unless otherwise noted)*

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Logic Level Input Voltage | $V_{BIAS}$ = 12 $V_{DC}$ (Note 8) | | | 0.5 | V |
| $V_{IH}$ | High Logic Level Input Voltage | $V_{BIAS}$ = 12 $V_{DC}$ (Notes 8, 9) | 2.4 | | | V |
| $V_{HYST}$ | Input Logic Threshold Hysteresis | $V_{BIAS}$ = 12 $V_{DC}$ | 0.2 | 0.4 | | V |
| $R_{IL}$ | Logic Input Pull-Down Resistance | $V_{BIAS}$ = 12 $V_{DC}$, $V_I$ = 5.0 $V_{DC}$ | | 10 | | kΩ |
| $C_{IL}$ | Logic Input Capacitance | $V_{BIAS}$ = 12 $V_{DC}$, $V_I$ → 5.0 $V_{DC}$ (Note 6) | | 6 | | pF |

### $V_{BIAS}$ and $V_{BOOT}$ Electrical Characteristics *(-55°C ≤ $T_C$ ≤ 125°C unless otherwise noted)*

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $I_{BIAS}$ | $V_{BIAS}$ Quiescent Operating Current | $V_{BIAS}$ = 12 $V_{DC}$, $B_{IN}$ = $T_{IN}$ = 0.5 $V_{DC}$ | | 22 | 25 | mA |
| | $V_{BIAS}$ Operating Current, $f_s$ = 1 MHz | $V_{BIAS}$ = 12 $V_{DC}$, D/C = 50% includes Iboot | | 32 | 45 | mA |
| $I_{BOOT}$ | $V_{BOOT}$ Quiescent Operating Current | ($V_{BOOT}$ - $V_{SN}$) = 12 $V_{DC}$, $T_{IN}$ = 0.5 $V_{DC}$ | | 8 | 11 | mA |
| | $V_{BOOT}$ Operating Current, $f_s$ = 1 MHz | ($V_{BOOT}$ - $V_{SN}$) = 12 $V_{DC}$, D/C = 50% | | 13 | 16 | mA |
| $V_{BOOT}$ | $V_{BOOT}$ - to - $V_{SN}$ Operating Voltage | ($V_{BOOT}$ - $V_{SN}$) = 12 $V_{DC}$ | 9 | 11.5 | 13 | V |

### Under-Voltage Lockout Static Electrical Characteristics *(-55°C ≤ $T_C$ ≤ 125°C unless otherwise noted)*

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{BIAS}$ UVLO+ | $V_{BIAS}$ UVLO Rising Threshold | (Note 10) | 5 | 9 | 10.9 | V |
| $V_{BIAS}$ (HYST) | $V_{BIAS}$ UVLO Falling Hysteresis | (Note 10) | | 0.6 | | V |
| $V_{BOOT}$ UVLO+ | $V_{BOOT}$ UVLO Rising Threshold | (Note 11) | 5 | 9 | 10.9 | V |
| $V_{BOOT}$ UVLO (HYST) | $V_{BOOT}$ UVLO Falling Hysteresis | (Note 11) | | 0.8 | | V |

### Low- and High-Side Power Switch Dynamic Electrical Characteristics *($T_C$ = 25°C unless otherwise noted)*

| Symbol | Parameter | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | $T_{IN}$-to-SN or $B_{IN}$-to-SN Turn-ON Delay Time | $V_{DS}$ = 25 $V_{DC}$; $I_O$ = 6A (See Switching Figures) | | 20 | 45 | ns |
| $t_{d(off)}$ | $T_{IN}$-to-SN or $B_{IN}$-to-SN Turn-OFF Delay Time | $V_{DS}$ = 25 $V_{DC}$; $I_O$ = 6A (See Switching Figures) | | 20 | 45 | ns |
| $t_r/t_f$ | SN Rise/Fall Time | $V_{DS}$ = 25 $V_{DC}$; $I_O$ = 6A (See Switching Figures) | | 3 | | ns |
| $t_{rl}/t_{fl}$ | Logic Input Rise/Fall Time | From $V_{IL}$ to $V_{IH}$ or $V_{IH}$ to $V_{IL}$ (Notes 6, 14) | | | 25 | ns |
| PW | Minimum $B_{IN}$/$T_{IN}$ Pulse Width | (Notes 6, 12, 13) | | 20 | | ns |
| $T_{(delay)}$ | $B_{IN}$-to-$T_{IN}$ or $T_{IN}$-to-$B_{IN}$ Dead (Delay) Time | (Notes 6, 12, 13) | 20 | | | ns |
| D/C | High-Side Power Switch Duty Cycle | (Notes 6, 12, 13) | | | 95 | % |
| $t_{prg}$ | High-Side Bootstrap Capacitor Pre-Charge Time | (Notes 6, 12, 13) | 5 | | | µs |
| $C_{OSS}$ | High Side Output Capacitance (VDD-SN) | V = 5 V (Note 6) | | 625 | | pF |
| | High Side Output Capacitance (VDD-SN) | V = 48 V (Note 6) | | 250 | | pF |
| | Low Side Output Capacitance (SN-PGND) | V = 5 V (Note 6) | | 625 | | pF |
| | Low Side Output Capacitance (SN-PGND) | V = 48 V (Note 6) | | 250 | | pF |

### Radiation Characteristics

EPC Space eGaN® ICs are tested according to MIL-PRF-38535 Method 1019 for total ionizing dose validation.

VBIAS = 12V
VDD = 60V
TIN = 0V-5V 40% DC 0° Phase
BIN = 0V-5V 40% DC 180° Phase

### Electrical Characteristics up to 300 krad *($T_C$ = 25°C)*

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $V_{DD}$ | Positive Power Supply Input Voltage (Note 1) | 60 | V |
| $I_{DD}$ | Continuous Operating Current | 6 | A |
| $V_{BIAS}$ | Continuous Gate Driver Bias Supply Voltage | 12 | V |
| $V_{BOOT}$ | Continuous Bootstrap Supply Voltage | 12 | |
| $B_{IN}$, $T_{IN}$ | $B_{IN}$ or $T_{IN}$ Logic Input Voltage | -0.3 to 5.5 | |

### Typical Single Event Effect Safe Operating Area

All radiation single event effects tests are performed in heavy ion environments such as the k-500 Cyclotron at Texas A&M. Transient events may occur at full rating but no burnout.

| Environment | | | VDD |
|---|---|---|---|
| Ion | LET MeV/mg/cm$^2$ | Fluence #/cm$^2$ | VBIAS = 12V |
| Bi | 61.13 | 1E+6 | 80V |

## Notes

1.) DC value of $V_{DD}$ plus any transient voltage spikes not to exceed this value.

2.) When either logic input ($B_{IN}$ or $T_{IN}$) is at the low input voltage level, the associated output switch is guaranteed to be OFF (high impedance).

3.) When either logic input ($B_{IN}$ or $T_{IN}$) is at the high input voltage level the associated output switch is guaranteed to be ON (low impedance) unless concurrent and therefore disabled by shoot-through protection.

4.) Measured using current pulse.

5.) Measured using 4-Wire (Kelvin) sensing techniques.

6.) Guaranteed by design. Not tested in production.

7.) Measured using 50 ns current pulse.

8.) Either $B_{IN}$ or $T_{IN}$ logic input.

9.) The input shoot-through protection is activated if both the $B_{IN}$ and $T_{IN}$ logic inputs are set to the logic high (“1”) condition simultaneously. In the case where the $B_{IN}$ and $T_{IN}$ inputs are set to logic high, both the low- and high-side power switches are set to their high impedance (OFF) state.

10.) Rising $V_{BIAS}$ levels below the $V_{BIAS}$ UVLO+ threshold and falling $V_{BIAS}$ levels below the $V_{BIAS}$ UVLO+ - $V_{BIAS}$ UVLO (HYST) threshold result in the internal low-side gate drivers being disabled and the corresponding output being set to its high- impedance state, regardless of the state of the logic input.

11.) Rising $V_{BOOT}$ levels below the $V_{BOOT}$ UVLO+ threshold and falling $V_{BOOT}$ levels below the $V_{BOOT}$ UVLO+ - $V_{BOOT}$ UVLO (HYST) threshold result in the internal high-side gate drivers being disabled and the corresponding output being set to its high- impedance state, regardless of the state of the logic input.

12.) The high-side power switch gate driver utilizes a bootstrap capacitor to provide the proper bias for this circuit. As such, this capacitor must be periodically re-charged from the $V_{BIAS}$ supply. The time $t_{prg}$ is the minimum time required to ensure that the bootstrap capacitor is properly charged when power is initially applied to the EPC7012L7BH IC.

13.) The minimum frequency of operation is determined by the external bootstrap capacitance and the bias current required by the high-side power switch gate driver circuit, $I_{BOOT}$. In order to keep the high-side power switch gate driver bootstrap capacitor properly charged on a cycle-by-cycle basis, it is recommended that the maximum duty cycle of the high-side power switch is limited to the value shown.

14.) See radiation reports for details.

## Switching Figures

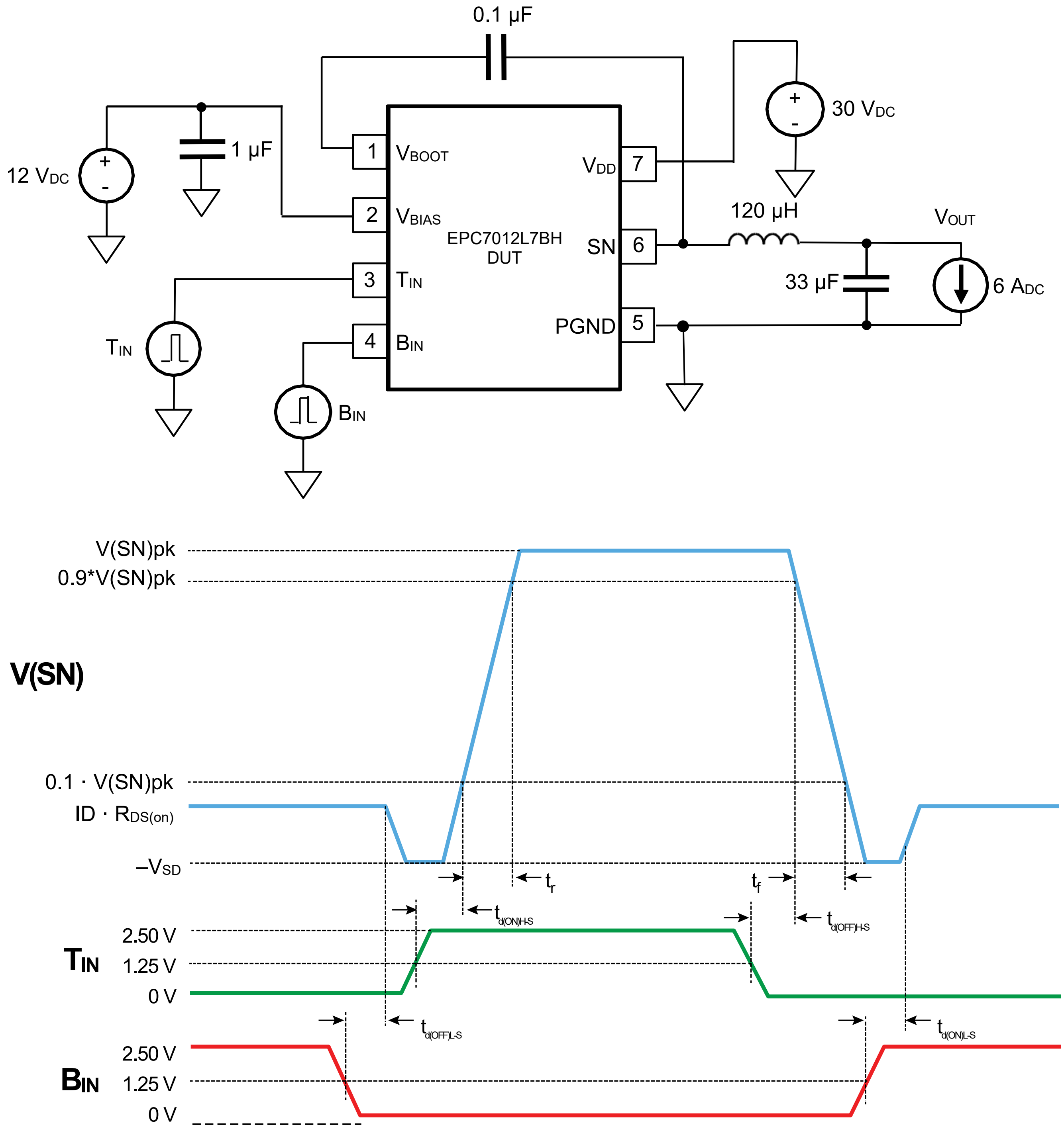



*Figure 1. Switching Figures*

| $B_{IN}$ | $T_{IN}$ | LS | HS |
|---|---|---|---|
| 0 | 0 | Off | Off |
| 1 | 0 | On | Off |
| 0 | 1 | Off | On |
| 1 | 1 | Off | Off |

## Logic Input Shoot- Through Protection

The EPC7012L7BH is provided with input shoot-through (cross-conduction) protection such that if the $B_{IN}$ and $T_{IN}$ logic inputs are asserted as logic state high ("1") simultaneously then the switching node (SN) assumes a high impedance (hi-Z) state until one of the logic inputs is asserted to a logic low ("0") state. This feature prevents the EPC7012L7BH IC from being destroyed by an unintentional logic condition at the logic inputs.

## High-Side Bootstrap Capacitor Periodic Recharge

The high-side power switch gate driver utilizes a bootstrap capacitor to provide the proper bias for this circuit during witching operation. As such, this capacitor must be periodically recharged from the $V_{BIAS}$ power supply. The time $t_{prg}$ is the minimum time required for the low-side driver to be turned ON in order to ensure that the bootstrap capacitor is properly charged when power is initially applied to the EPC7012L7BH IC.

## Power-Up Sequencing

There are no power sequencing requirements for the $V_{BIAS}$ and $V_{DD}$ power supplies required by the EPC7012L7BH. The two power supplies may be applied to the IC in any order/sequence required by the end-user.

## Schottky "Freewheeling" Diodes

If third-quadrant operation of the internal output HEMTs in the EPC7012L7BH is not desired, then it is recommended that two external Schottky "Freewheeling" diodes (Dext1 and Dext2) be added between VDD and SN and between SN and PGND as shown in Figure 2. The diodes should be properly de-rated for both voltage and current.

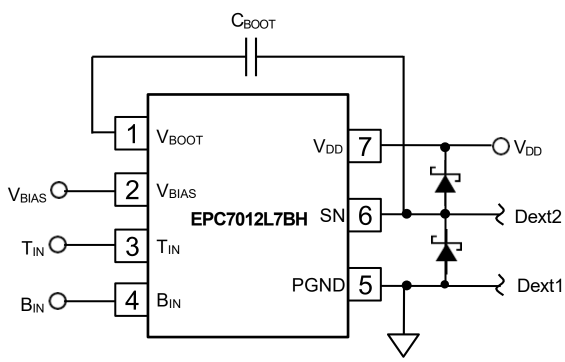



*Figure 2. External Schottky Freewheeling Diode Connections*

Place the diode packages as physically close to the EPC7012L7BH package as possible, and keep the connections as short as possible, to eliminate parasitic loop inductances.

## Resistors on Decoupling Capacitors

The EPC7012L7BH is designed to be a high-speed power driver. As such it has extremely fast switching node (SN) rise and fall times by design. Fast rise and fall times can and will result in unwanted voltage spikes at the $V_{DD}$ and PGND pins due to any parasitic layout inductance ($V_{SPIKE} = L_{Par} \cdot dI / dt$). If these spikes cannot be reduced to an acceptable level through PCB optimization, two resistors may be added to provide the necessary damping to the local supply loop. These resistors, $R_{SD1}$ and $R_{SD2}$ are shown in Figure 3.

$R_{SD1}$ increases the fall time of the SN, as it affects the low side driver. Similarly, $R_{SD2}$ increases the SN rise time. It is recommended to minimize the value of these resistors to the minimum necessary to obtain the desired loop damping.

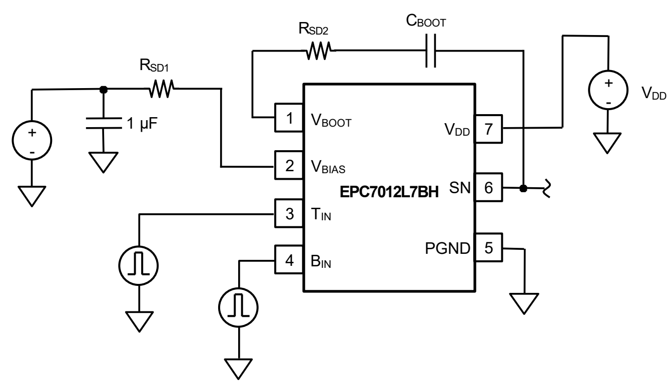



*Figure 3. External Damping Resistor Connections*

## Recommended VDD-to-PGND Power Supply Bypassing

The $V_{DD}$ power supply pin and the return pin of the EPC7012L7BH require proper high frequency bypassing.

Because of the extremely high slew-rate of voltage seen at the SN output it is recommended that a minimum of one (1) 3.3 μF microfarad ceramic capacitor, one (1) 1.0 microfarad ceramic capacitor, one (1) 0.1 microfarad ceramic capacitor and one (1) 0.01 microfarad ceramic capacitor, all with sufficient voltage de-rating, be connected from $V_{DD}$ to PGND. All four of these capacitors should be low ESR types, if possible. It is strongly recommended that these capacitors have the smallest possible case sizes possible such that they inscribe the smallest possible loop area between $V_{DD}$ and PGND so as to minimize the inductance related to this loop area. Also, to reduce the inductive loop between $V_{DD}$ and PGND is strongly recommended that an induction loop cancellation layout of the high frequency power supply capacitors be employed. Figure 4 illustrates the recommended optimum layout and placement for the $V_{DD}$-PGND high-frequency bypass capacitors.

It should be noted that in Figure 4 that the light green copper etch area on the PCB's inner layer #1 is positioned directly beneath the copper etch clad on the top layer, as indicated by the dashed line.

The recommended component placement and etch layout capitalize upon the magnetic field cancellation between adjacent current carrying layers on the PCB. The high-frequency AC current (shown in **RED** in the side view) drawn from the $V_{DD}$ power bus through the EPC7012L7BH IC is then returned through the adjacent PCB copper etch layer with the same amplitude in the opposite direction, with the effect of mutually cancelling the induced field. The result is a very small residual parasitic loop inductance, and an associated lower spike voltage present on the $V_{DD}$ and PGND pins of the IC.

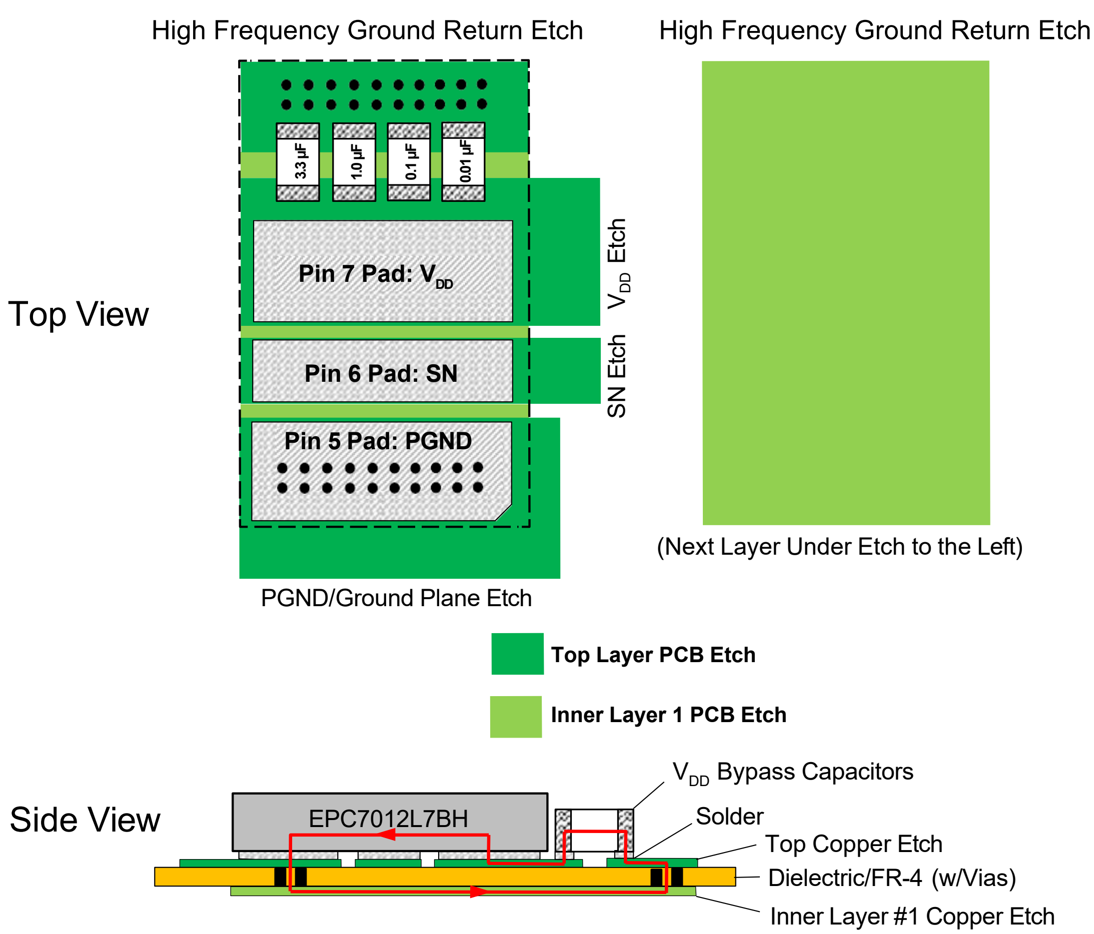



*Figure 4. Recommended Optimum $V_{DD}$-to-PGND Power Supply Bypass Capacitor Layout (Not to Scale)*

## Suggested Schematic Symbol

The suggested schematic symbol for the EPC7012L7BH is shown in figure 5.

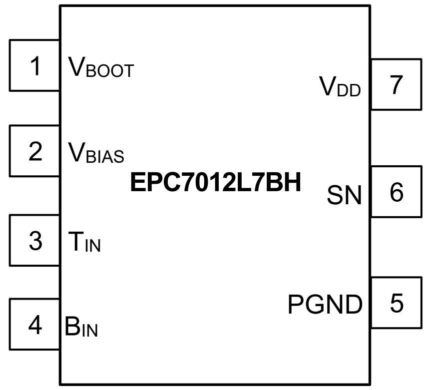



Figure 5. Suggested EPC7012L7BH Integrated Circuit Schematic Symbol

## Typical Application Information

In all the following figures only the pins that are considered or that require connection are identified

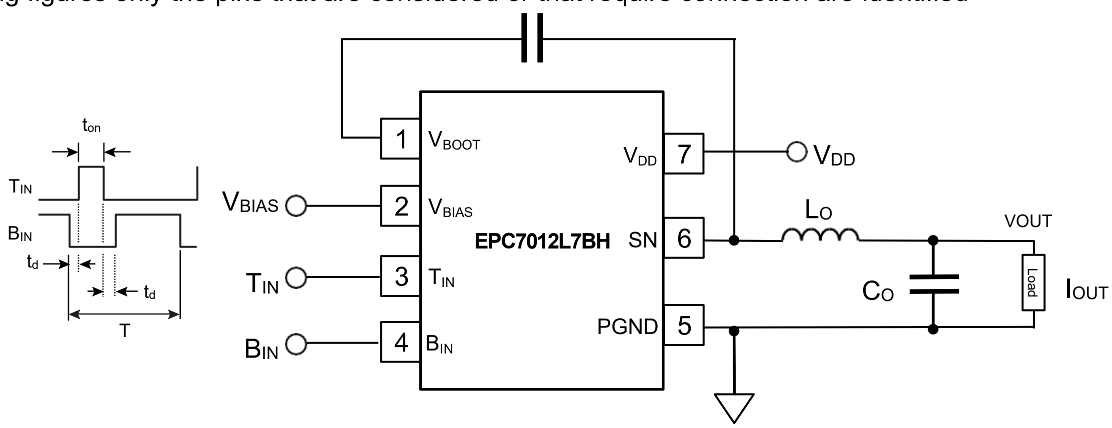



*Figure 6. Low Parts-Count POL Converter Power Output Stage*

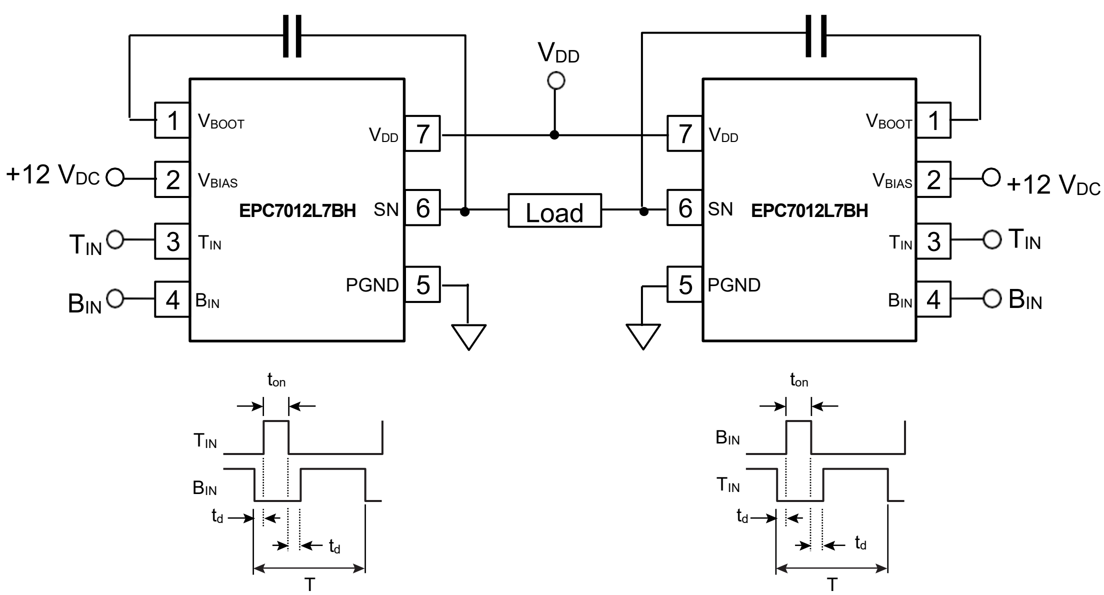
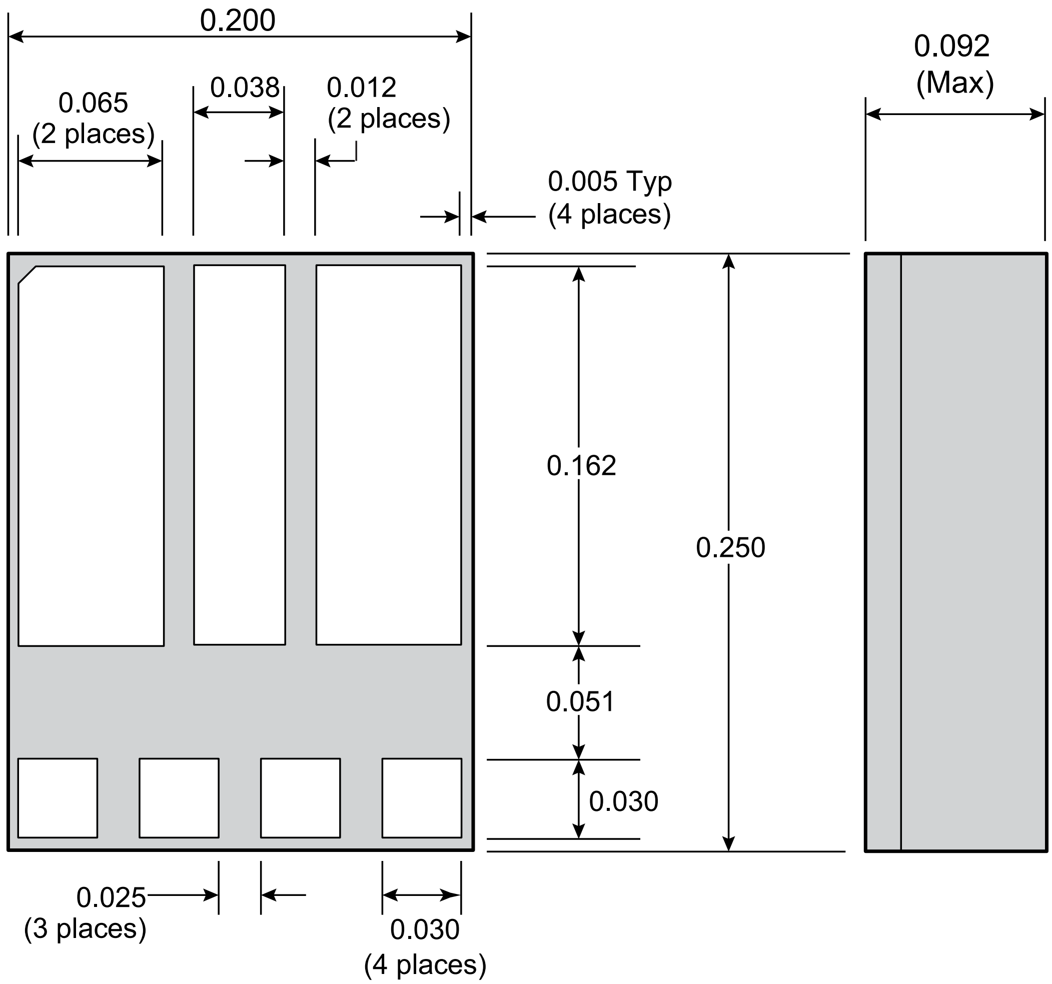



*Figure 7. Full Bridge Power Output Stage.*

## Package Outline and Dimensions




Note: All dimensions are in inches

**ALL tolerances +/- 0.005**

*Figure 8. EPC7012L7BH Package Outline and Dimensions*

## Recommended PCB Solder Pad Configuration

It is important that the EPC7012L7BH package be soldered to the PCB motherboard using SN63 (or equivalent) solder. Care should be taken during processing to ensure there is minimal solder voiding in the contacts to the $V_{DD}$ (pin 7), SN (pin 6) and PGND (pin 5) pads on the package. The recommended pad dimensions and locations are shown in Figure 9. All dimensions are shown in inches.

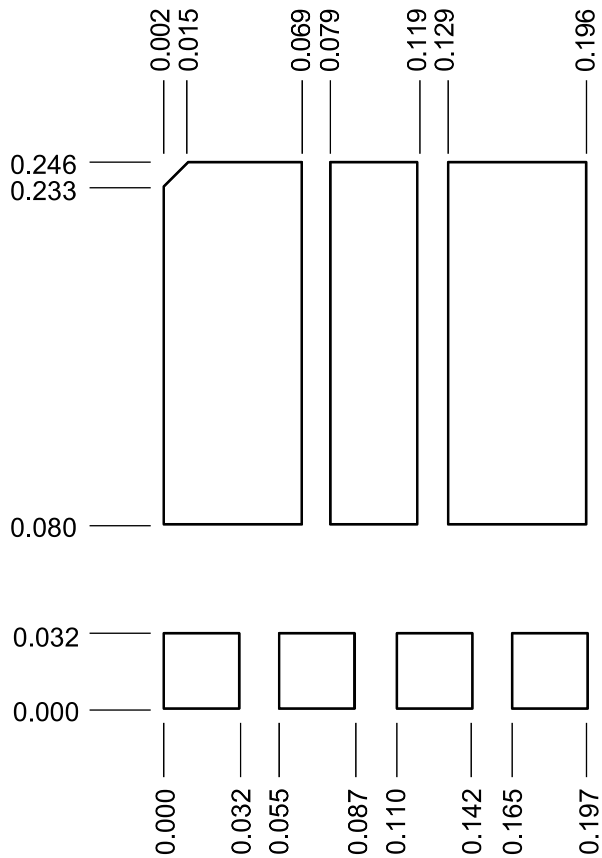



*Figure 9. Recommended PCB Solder Pad Configuration (Top View)*

## Example Typical Reflow Profile

The profile shown in Figure 10, below, is a typical reflow profile example. Optimize target reflow temperature profiling based on the actual solder paste used. The peak case temperature of the EPC7012L7BH should never exceed 260°C.

EPC Space assumes no liability in conjunction with the use of this profile recommendation.

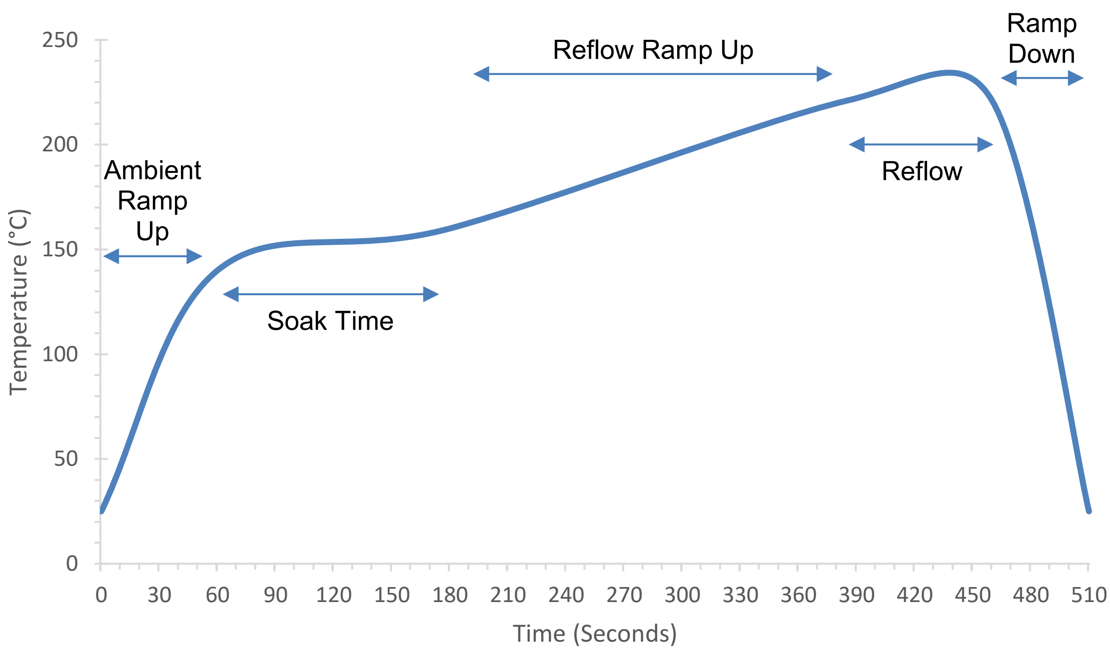



*Figure 10. Typical Package SN63/37 Solder Attachment Reflow Profile*

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