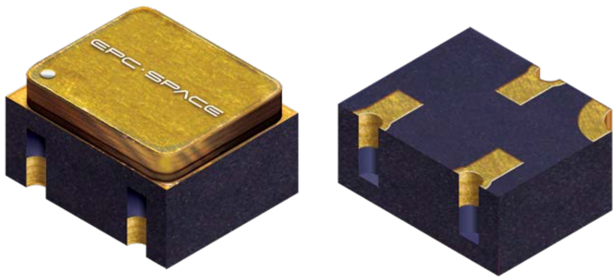
Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- No Wire Bond for Higher Reliability and Low Inductance
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 84 MeV/(mg/cm^2) with V_{DS} up to 100% of rated Breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 4 x 10^{15} Neutrons/cm^2

Application

- Commercial Satellite EPS & Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities



EPC7014UBC

Rad-Hard eGaN® 60 V, 1 A, 580 mΩ Surface Mount (UB)

Description

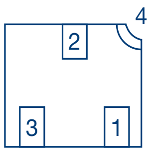
EPC Space Rad-Hard eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{θJA}$	Thermal Resistance Junction to Ambient (Note 3)	200	°C/W
$R_{θJC}$	Thermal Resistance Junction to Case	35	

I/O Pin Assignment *(Bottom View)*

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	L	Lid Pad Connection



Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	60	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72	
I_D	Continuous Drain Current ID @ V_{GS} = 5 V, T_C = 25°C	1	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} \le$ 80 µs	4	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1A(ΔA)	
Weight	Device Weight	0.058	g

Electrical Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V		60			V
Drain to Source Leakage	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	T_C = 25°C		0.17	100	µA
			T_C = 125°C		0.35	180	µA
Gate to Source Forward Leakage	I_{GSSF}	V_{GS} = 5 V	T_C = 25°C		2	500	µA
Gate to Source Reverse Leakage	I_{GSSR}	V_{GS} = -3 V	T_C = 25°C		0.27	100	µA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 0.14 mA	T_C = 25°C	0.8	1.8	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T$	V_{DS} = V_{GS} , I_D = 0.14 mA	-55°C < T_A < 150°C		|2.34|		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	I_D = 1 A, V_{GS} = 5 V	T_C = 25°C		340	580	mΩ
Source to Drain Forward Voltage	V_{SD}	I_S = 0.5 A, V_G = 0 V	T_C = 25°C		2.5	3	V

Dynamic Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 30 V, V_{GS} = 0 V		18	22	pF
Output Capacitance	C_{OSS}	V_{DS} = 30 V, V_{GS} = 0 V		17	30	pF
Reverse transfer Capacitance	C_{RSS}	V_{DS} = 30 V, V_{GS} = 0 V		0.1	2	pF
Gate Resistance (Note 5)	R_G	f = 1 MHz, V_{DS} = V_{GS} = 0 V		12.6		Ω
Total Gate Charge (Note 6)	Q_G	V_{DS} = 30 V, I_D = 0.5 A		142	184	pC
Gate to Source Charge (Note 6)	Q_{GS}	V_{DS} = 30 V, I_D = 0.5 A		20	35	pC
Gate to Drain Charge (Note 6)	Q_{GD}	V_{DS} = 30 V, I_D = 0.5 A		30	50	pC
Output Charge (Note 5)	Q_{OSS}	V_{GS} = 0 V, V_{DS} = 30 V		764	1145	
Source to Drain Recovery Charge (Note 5)	Q_{RR}	I_D = 1 A, V_{DS} = 30 V		0		

Figure 1: Typical Gate-Source Leakage Current vs. Ambient Temp.

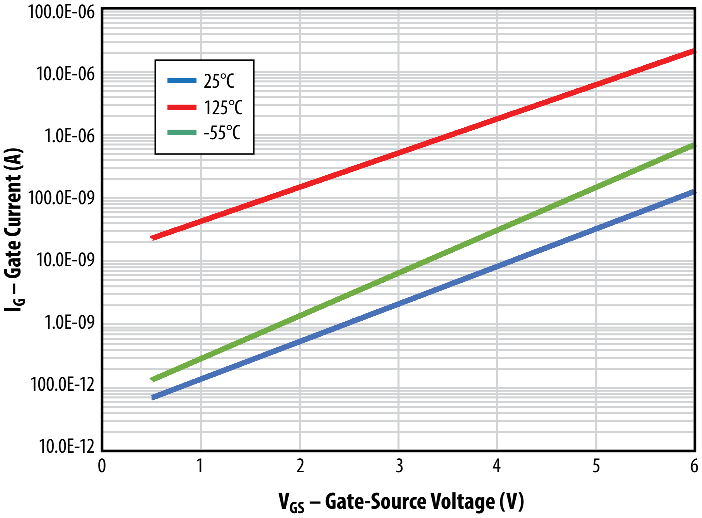


Figure 2: Typical Drain-Source Leakage Current vs. Ambient Temp.

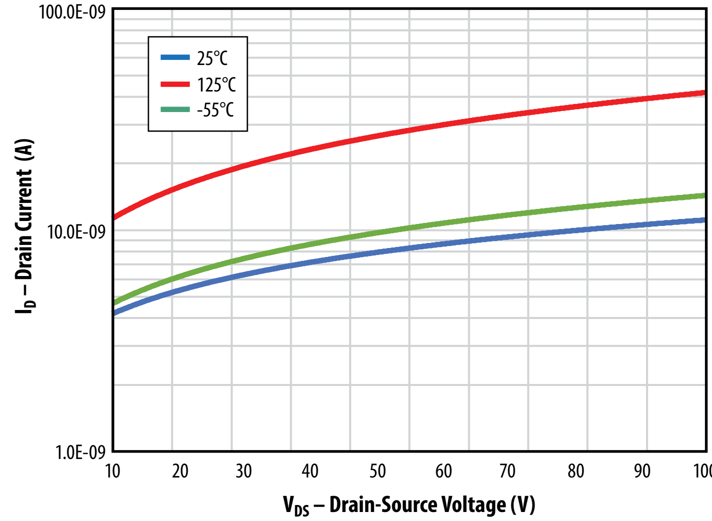


Figure 3: Typical Output Characteristics at 25°C

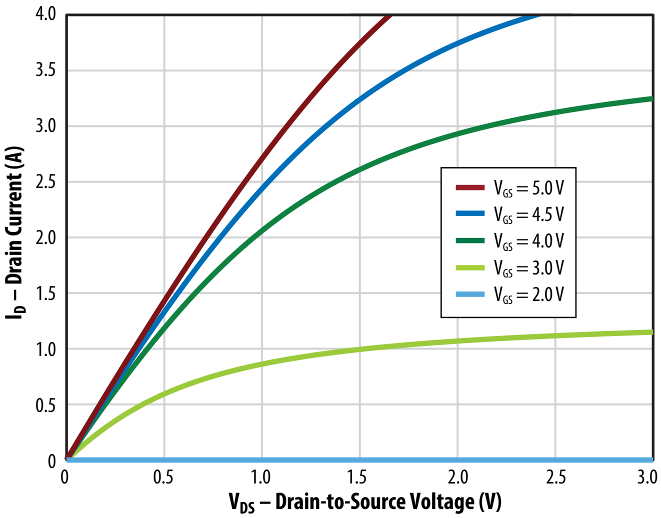


Figure 4: Typical Output Characteristics at 25°C

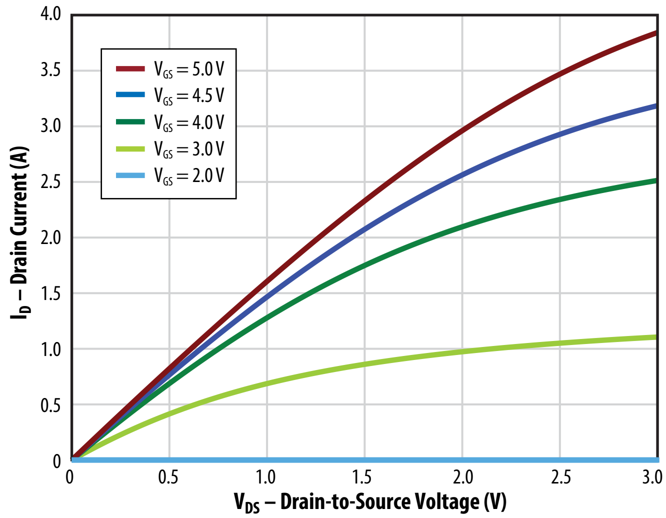


Figure 5: Transfer Characteristics

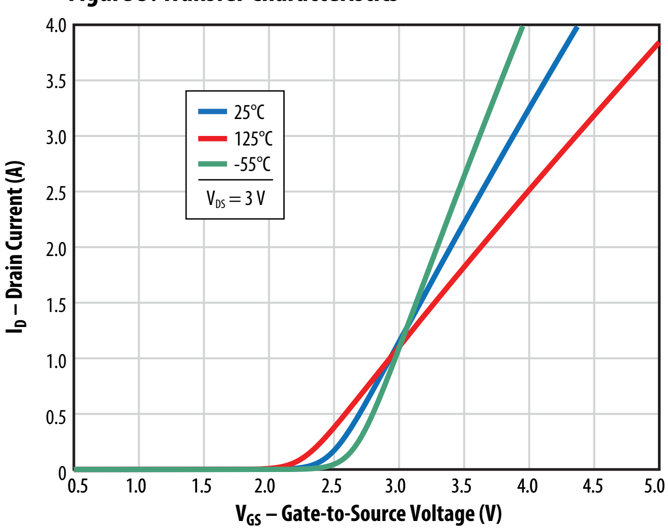


Figure 6: Reverse Drain-Source Characteristics

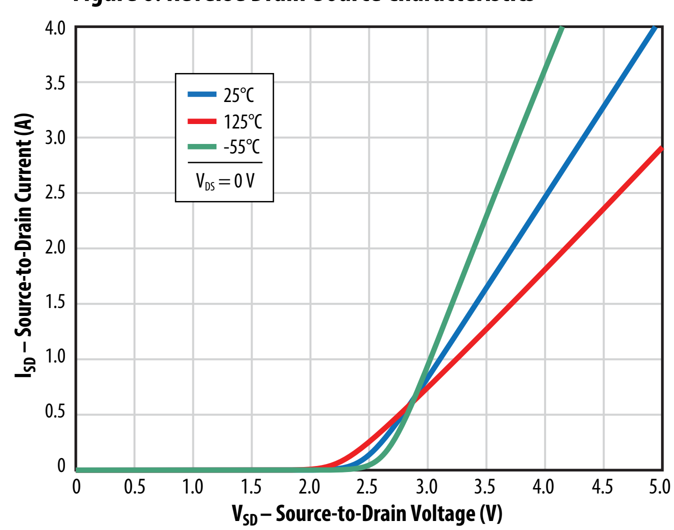


Figure 7: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

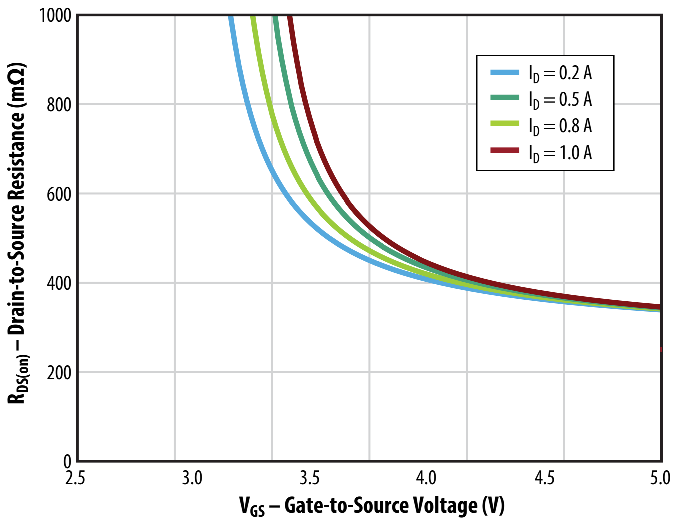


Figure 8: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

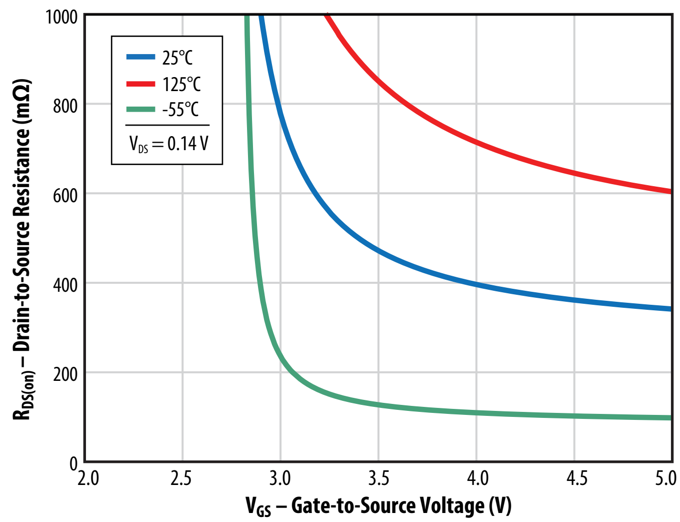


Figure 9: Normalized On-State Resistance vs. Temperature

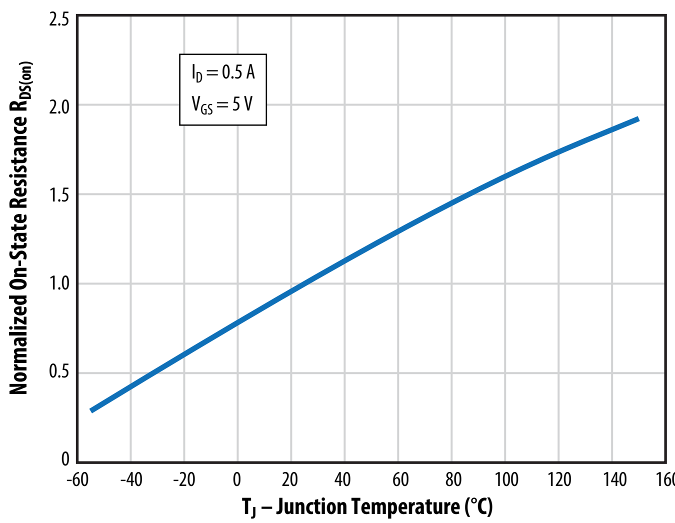


Figure 10: Normalized Threshold Voltage vs. Temperature

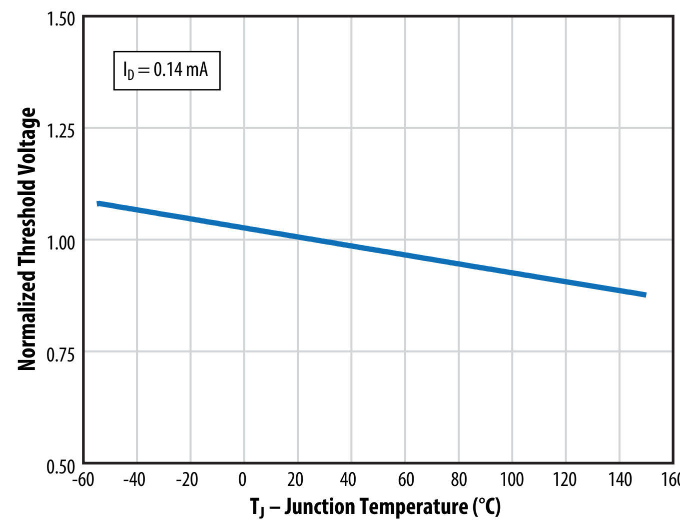


Figure 11: Capacitance (Linear Scale)

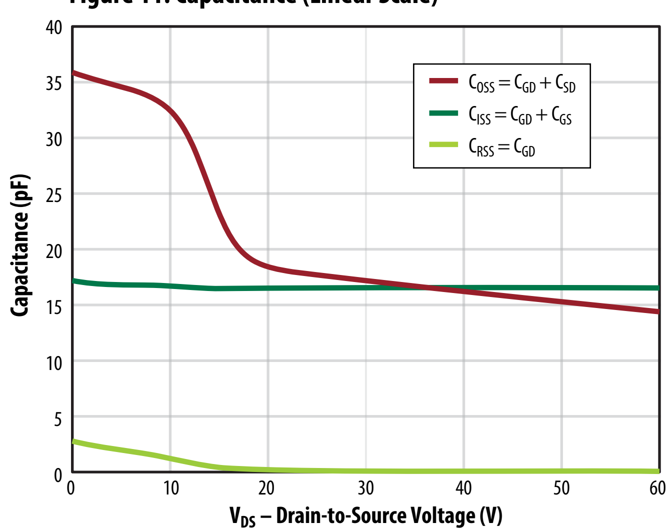


Figure 12: Output Charge and C_{OSS} Stored Energy

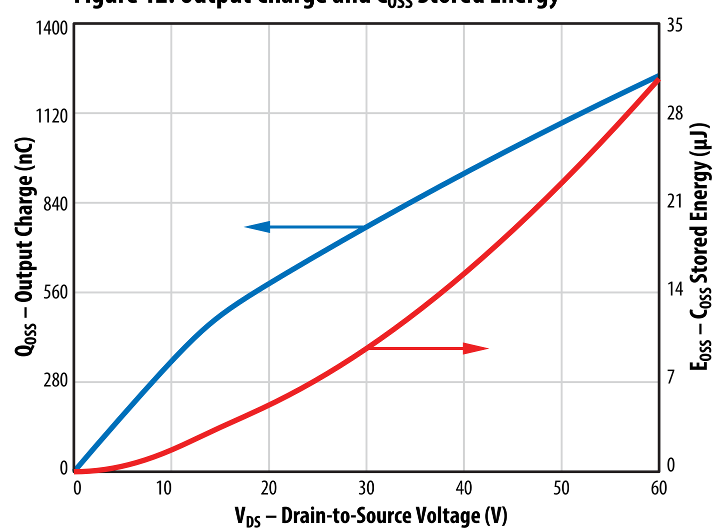


Figure 13: Gate Charge

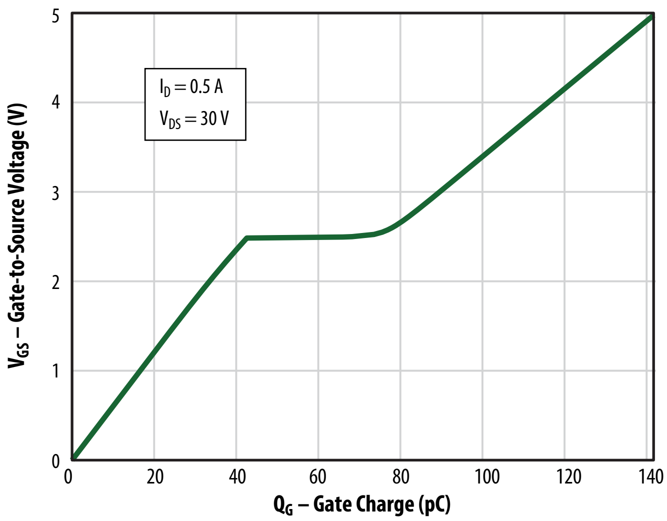


Figure 14: Safe Operating Area

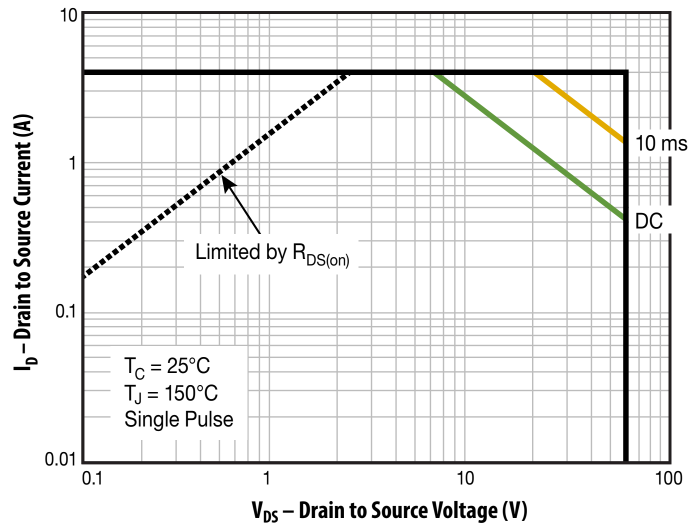
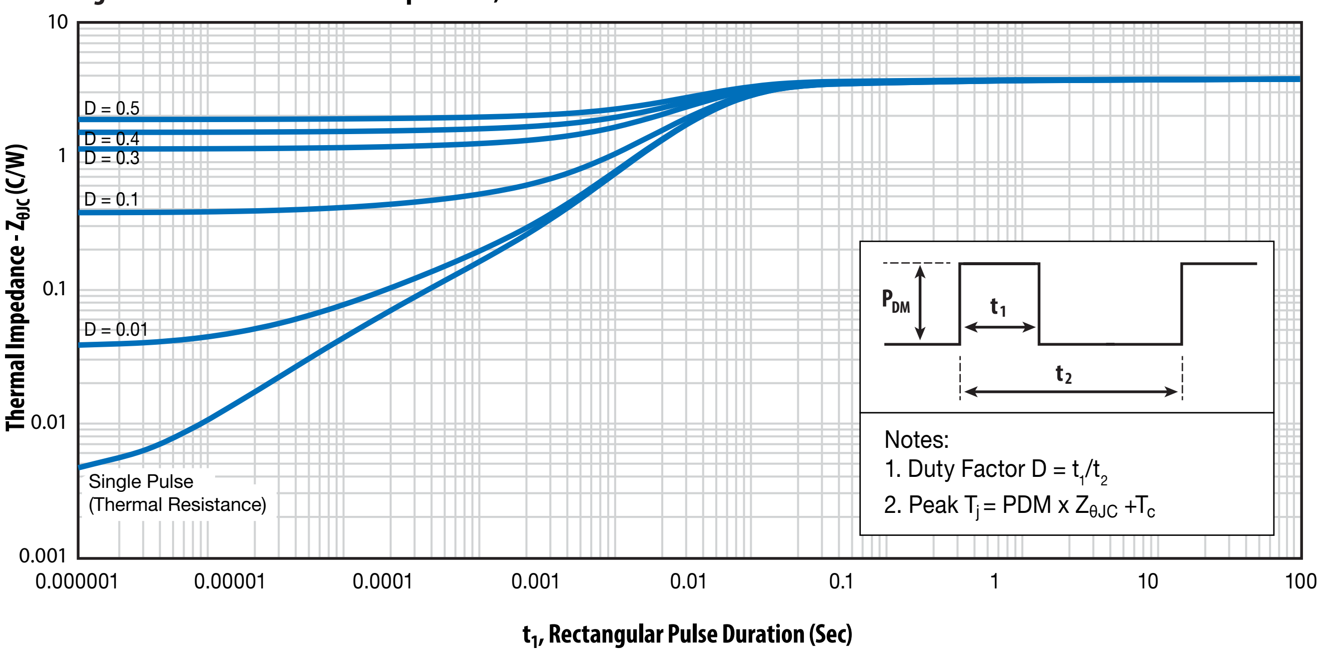
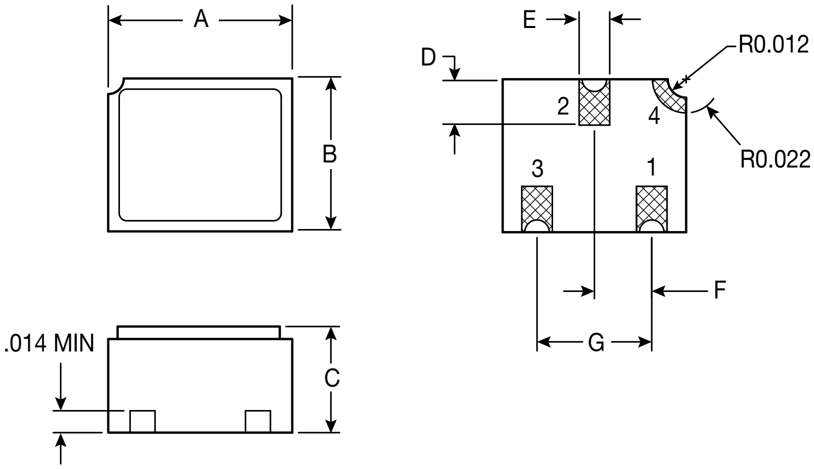


Figure 15: Transient Thermal Impedance, Junction-to-Case



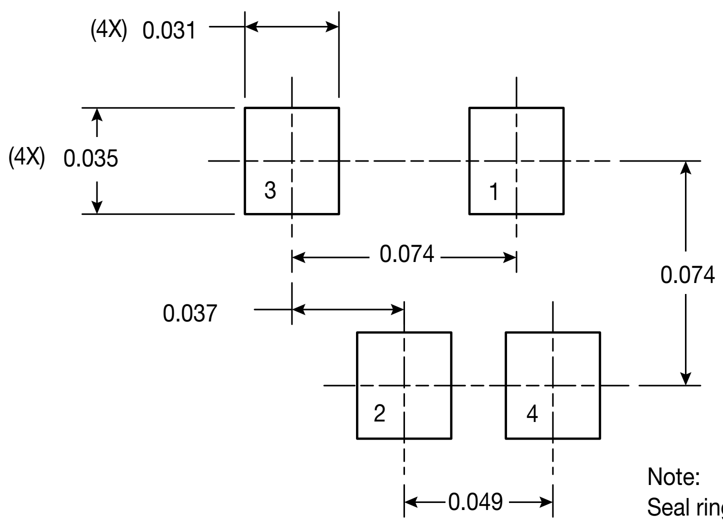
Package Outline and Dimensions



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.115	0.128	2.921	3.251
B	0.095	0.108	2.413	2.743
C	0.064	0.082	1.625	2.083
D	0.024	0.036	0.610	0.910
E	0.016	0.024	0.410	0.610
F	0.035	0.039	0.889	0.991
G	0.071	0.079	1.803	2.006

Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb.

UB Footprint for Printed Circuit Board Design



Note:
Seal ring/lid ground optional (pin/pad 4)

Notes

Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5V for optimum operation across life and radiation.

Note 3. $R_{\theta JA}$ measured with LCC3 package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 5. Guaranteed by design/device construction. Not tested.

Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

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