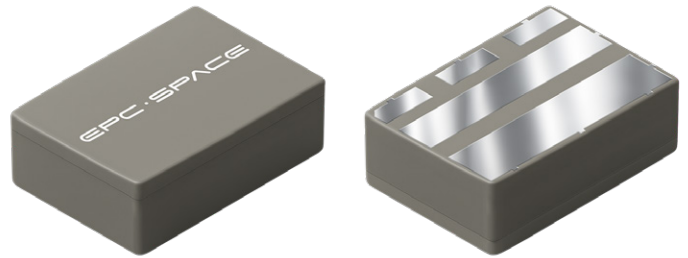


Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
Dual Gate
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune



EPC7018GC

**Rad-Hard eGaN® 100 V, 80 A,
6.0 mΩ Surface Mount (FSMD-G)**

Description

EPC Space FSMD-G series of eGaN® power switching HEMTs have been specifically designed for critical applications in the high reliability or commercial satellite space environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Applications

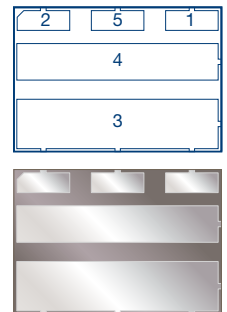
- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	45	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.84	

I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	G	Gate
3	D	Drain
4	S	Source
5	SS	Source Sense



Absolute Maximum Rating ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous Drain Current I_D @ $V_{GS} = 5\text{ V}$	80	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} = 300\ \mu\text{s}$	320	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{SOL}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1B (ΔB)	
Weight	Device Weight	0.170	g

Static Characteristics (Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units	
Drain to Source Voltage	B_{VDSS}	$V_{GS} = 0\text{ V}$	100			V	
Drain to Source Leakage	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		0.002	0.4	mA	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	$T_C = 125^\circ\text{C}$	0.05	0.8		
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 6\text{ V}$		0.009	0.6	mA	
Gate to Source Forward Leakage		$V_{GS} = 6\text{ V}$	$T_C = 125^\circ\text{C}$	0.035	1		
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4\text{ V}$		0.001	0.5		
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 18\text{ mA}$	$T_C = 25^\circ\text{C}$	0.8	1.65	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}$		$-55^\circ\text{C} < T_A < 150^\circ\text{C}$		1.0		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$V_{GS} = 5\text{ V}, I_D = 80\text{ A}$	$T_C = 25^\circ\text{C}$	4	6	mΩ	
Source to Drain Forward Voltage	V_{SD}	$I_S = 0.5\text{ A}, V_G = 0\text{ V}$	$T_C = 25^\circ\text{C}$	1.8	3	V	

Dynamic Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1700	2100	pF
Reverse transfer Capacitance	C_{RSS}			1.2	6	
Output Capacitance	C_{OSS}			914	1050	
Total Gate Charge (Note 6)	Q_G	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 80\text{ A}$		11.7	20	nC
Gate to Source Charge (Note 6)	Q_{GS}			4.0	7	
Gate to Drain Charge (Note 6)	Q_{GD}			2.1	12	
Output Charge (Note 5)	Q_{OSS}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		63		
Source to Drain Recovery Charge (Note 5)	Q_{RR}			0		

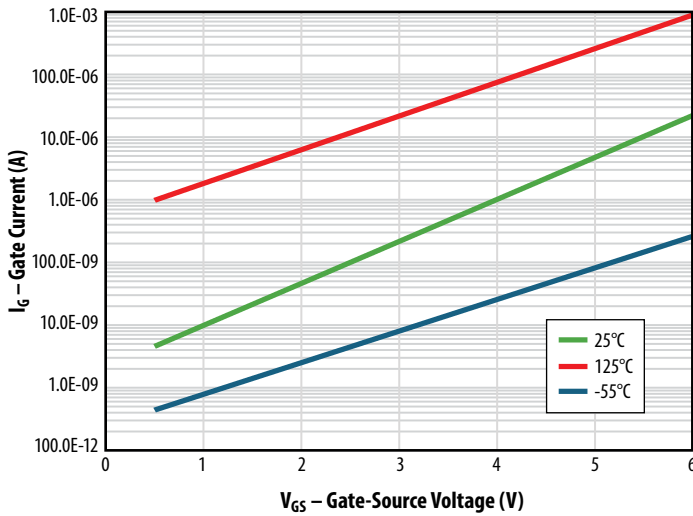


Figure 1: Typical Gate-Source Leakage Current vs. Ambient Temperature

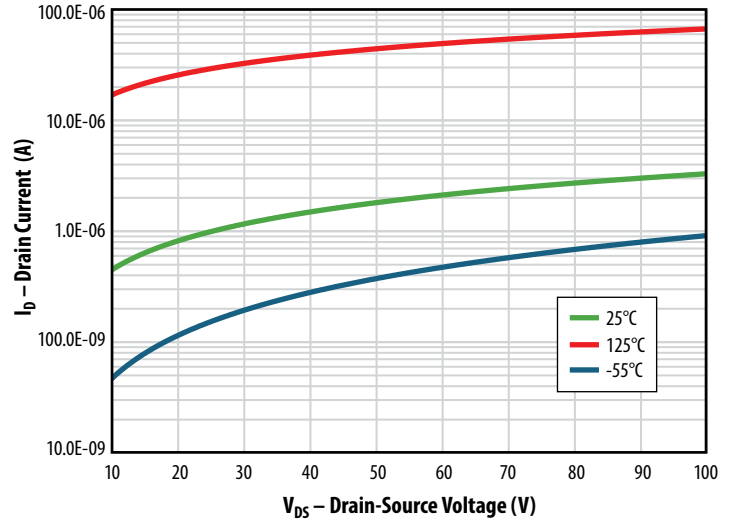


Figure 2: Typical Drain-Source Leakage Current vs. Ambient Temperature

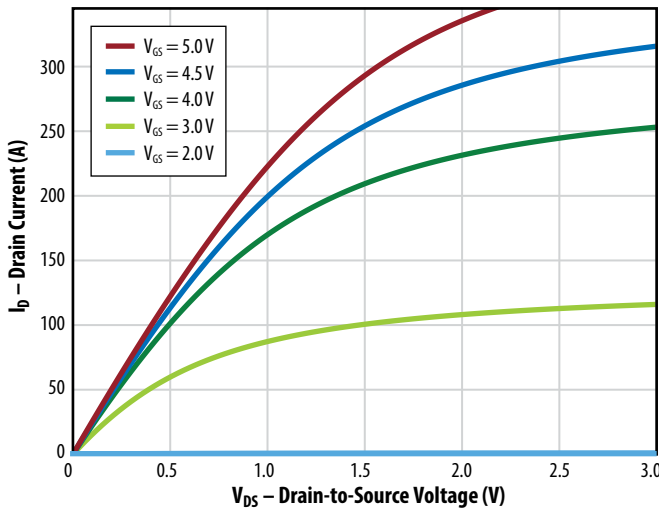


Figure 3: Typical Output Characteristics at 25°C

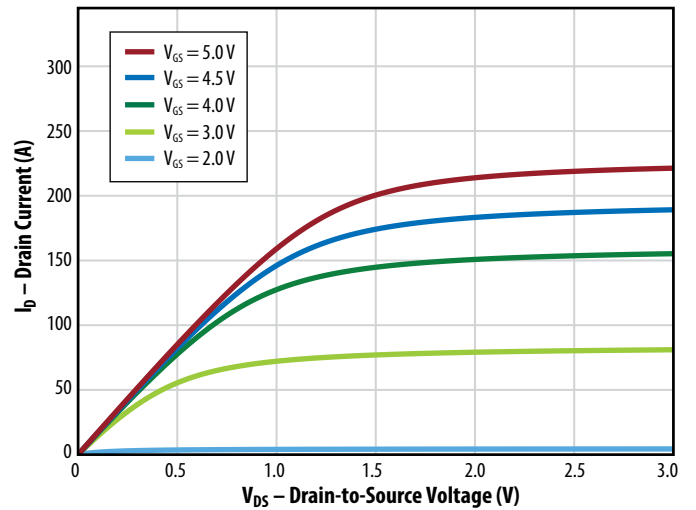


Figure 4: Typical Output Characteristics at 125°C

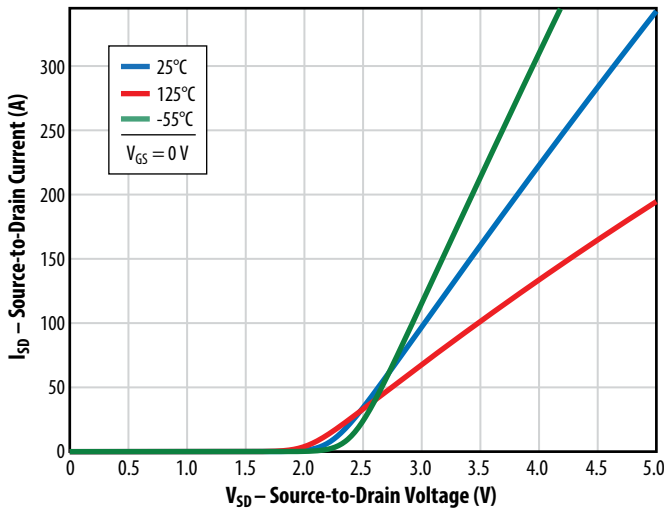


Figure 5: Reverse Drain-Source Characteristics

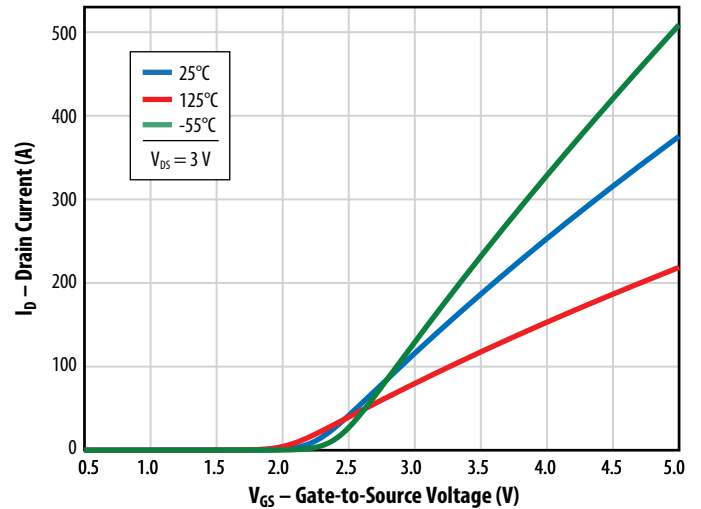


Figure 6: Typical Transfer Characteristics

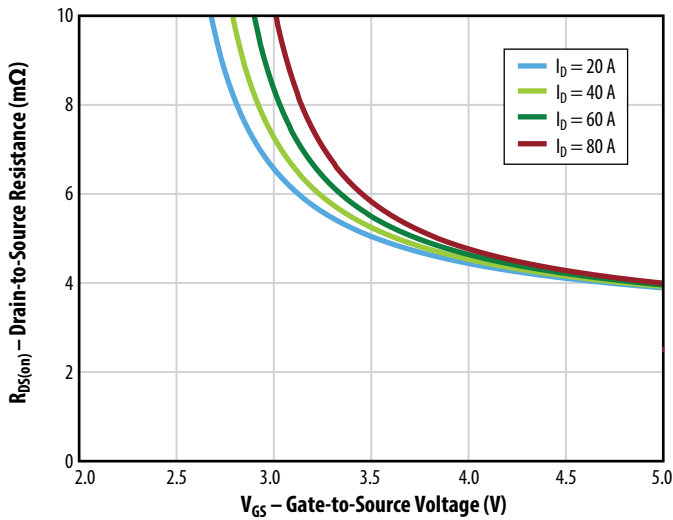


Figure 7: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

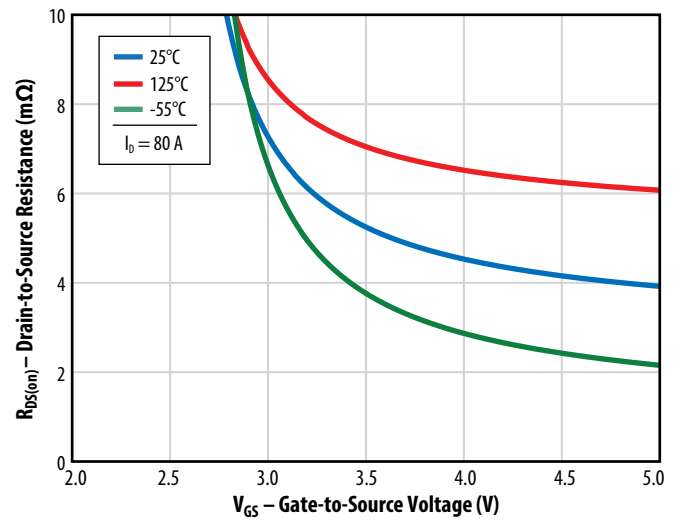


Figure 8: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

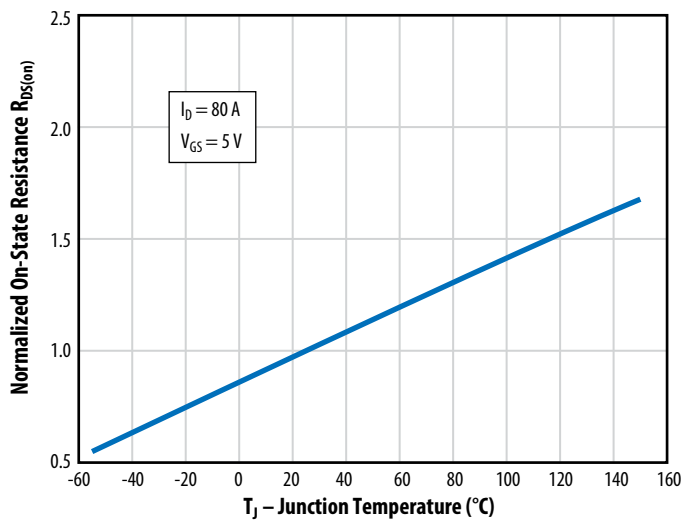


Figure 9: Normalized On-State Resistance vs. Temperature

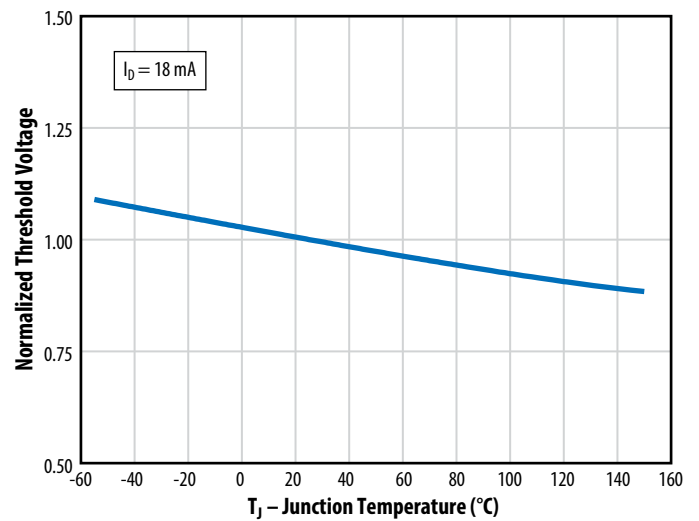


Figure 10: Normalized Threshold Voltage vs. Temperature

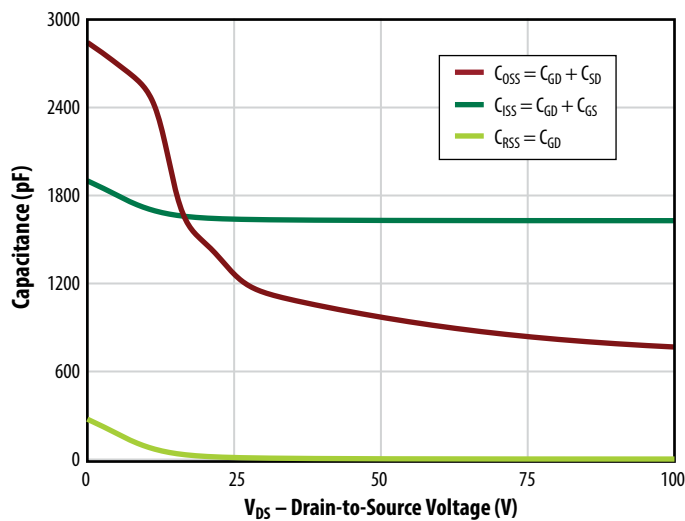


Figure 11: Typical Capacitance (Linear Scale)

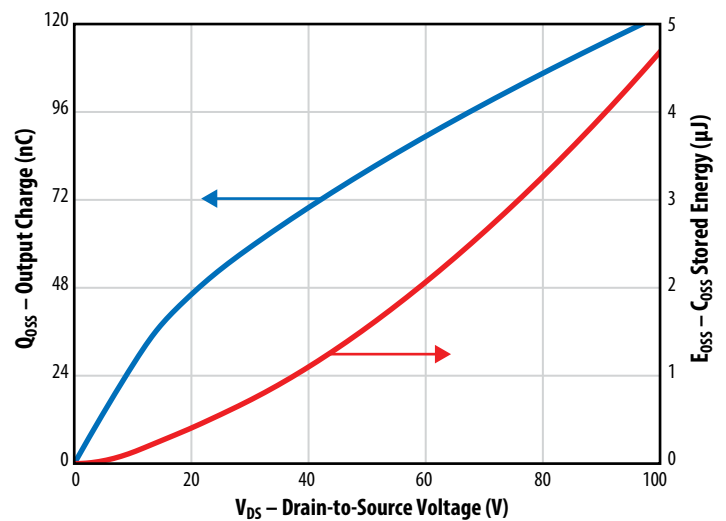


Figure 12: Output Charge and C_{OSS} Stored Energy

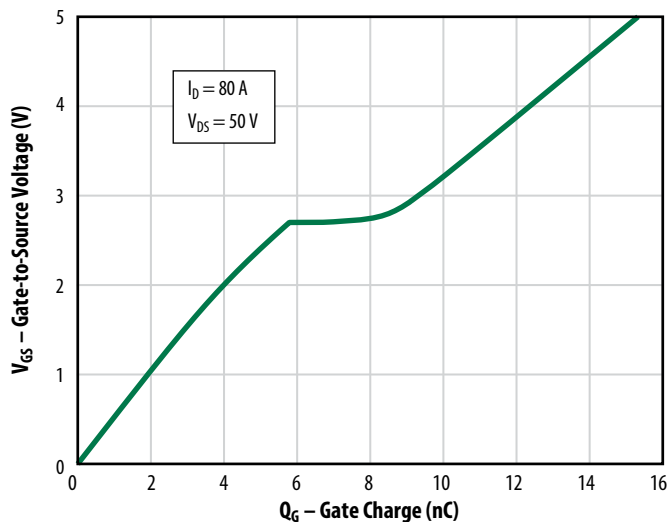


Figure 13: Gate Charge



Figure 14: Safe Operating Area

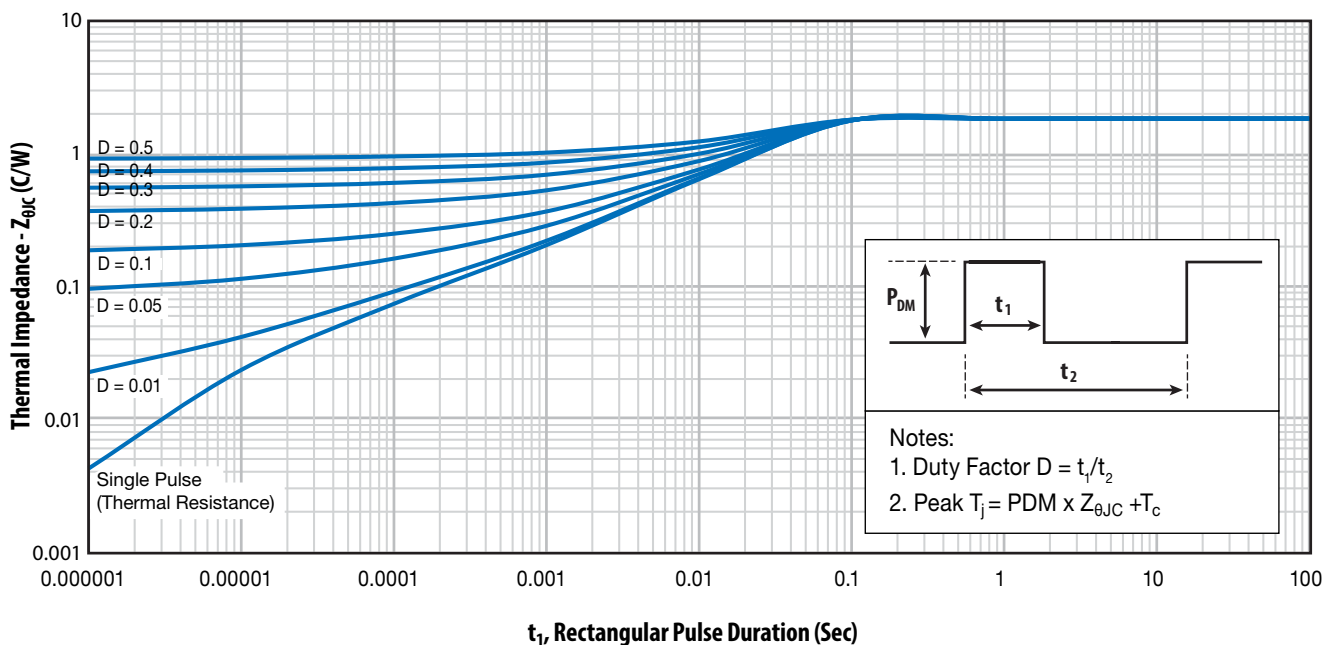
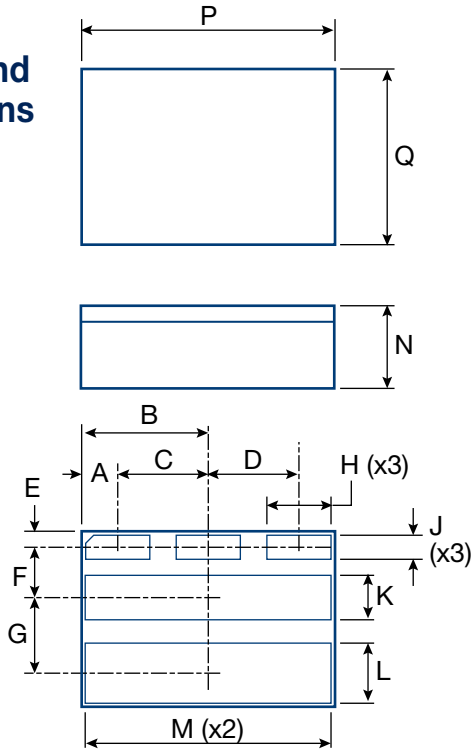


Figure 15: Transient Thermal Impedance, Junction-to-Case

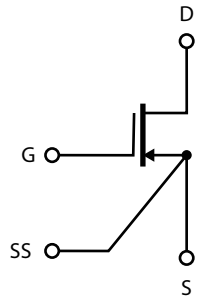
Package Outline and Dimensions



Symbol	IN		MM	
	NOM	REF	NOM	REF
A		0.045		1.14
B		0.158		4.01
C	0.113		2.87	
D	0.113		2.87	
E		0.020		0.51
F	0.063		1.6	
G	0.094		2.39	
J	0.03		0.76	
K	0.056		1.42	
L	0.070		1.78	
M	0.307		7.8	
N		0.083		2.11
P	0.315		8	
Q	0.219		5.56	

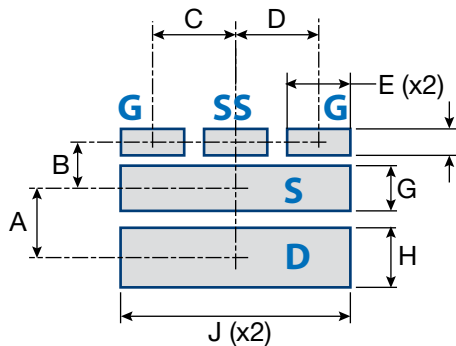
Note: All dimensions have a tolerance of ± 0.005 in [± 0.13 mm]
 Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb

Package Connections



NOTE: SS pin is connected directly to source of internal die.

FSMD-G Footprint for Printed Circuit Board Design



Symbol	IN	MM	Note
	NOM	NOM	
A	0.094	2.39	
B	0.063	1.6	
C	0.113	2.87	
D	0.113	2.87	
E	0.083	2.11	
F	0.036	0.91	
G	0.063	1.60	
H	0.081	2.06	
J	0.313	7.95	

Suggested footprint:
 NOM. DIM = .003 in [0.08 mm] swell on average

Notes

- Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5V for optimum operation across life and radiation.
- Note 3. $R_{\theta JA}$ measured with FSMD-G package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 μ s and duty cycle is 1%, maximum.
- Note 5. Guaranteed by design/device construction. Not tested.
- Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S . The gate current is adjusted to yield the desired charge per unit time ($I_{const} \cdot \text{time per division}$) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off}/t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC} .

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