Features

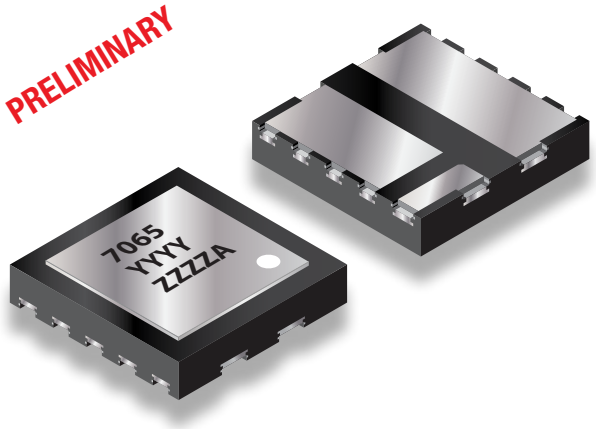
- Screened to Space Level
- Moisture Rating MSL1
- Ultra Low $R_{DS(on)}$
- Ultra-low Q_G For High Efficiency
- Ultra-low $R_{DS(on)}$ x Q_G and $R_{DS(on)}$ x Q_{OSS} FOMs
- Ideal for IBC and IVR/POL Applications
- No reverse recovery
- PQFN Package with Backside Thermal Pad
- Total Ionizing Dose HDR/LDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 83.2 MeV/(mg/cm^2) with V_{DS} up to 100% of rated breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 4 x 10^{15} Neutrons/cm^2

Applications

- High Performance, high power-density DC-DC Conversion
- High-Frequency DC-DC Converters
- Synchronous Rectifiers

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	0.9	



EPC7065PCSH

eGaN® FET in a Plastic Surface Mount 40 V, 101 A, 0.5 mΩ

Description

EPC's eGaN® power switching HEMTs have been specifically designed for critical applications in DC-DC conversion. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging. EPC7065PCSH has been specifically designed for synchronous rectifier applications on the secondary side of a 48 V-12 V LLC converter, where it brings an industry leading low R_{on} x Q_G figure of merit and enables higher frequency and higher efficiency operation.

Maximum Rating

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain-to-Source Voltage (Note 1)	40	V
$V_{DS(tr)}$	Drain-to-Source Voltage (Repetitive Transient)[1]	48	
I_D	Continuous ($T_J \leq 125°C$)	101	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	553	
V_{GS}	Gate-to-Source Voltage (Note 2)	+6 / -4	V
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

[1] Pulsed repetitively, duty cycle factor (DC_{Factor}) ≤ 1%;
See Figure 13 and **Reliability Report Phase 16**, Section 3.2.6

Static Characteristics *(T_J = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 0.5 mA	40			V
Drain to Source Leakage	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		0.2		
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 5 V		0.085		mA
Gate to Source Forward Leakage		V_{GS} = 5 V, T_J = 125°C				
Gate to Source Reverse Leakage		V_{GS} = -2 V		0.3		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 20 mA	0.8	1.2	2.5	V
Drain to Source On Resistance (Note 3)	$R_{DS(on)}$	V_{GS} = 5 V, I_D = 20 A		0.5		mΩ
Source to Drain Forward Voltage	V_{SD}	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

Dynamic Characteristics# *(T_J = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 20 V, V_{GS} = 0 V		4520		pF
Reverse Transfer Capacitance	C_{RSS}			30		
Output Capacitance	C_{OSS}			991		
Effective Output Capacitance, Energy Related (Note 4)	$C_{OSS(ER)}$	V_{DS} = 0 to 20 V, V_{GS} = 0 V		1196		
Effective Output Capacitance, Time Related (Note 5)	$C_{OSS(TR)}$			1487		
Total Gate Charge (Note 6)	Q_G	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 20 A		26		nC
Gate to Source Charge (Note 7)	Q_{GS}	V_{DS} = 20 V, I_D = 20 A		7.5		
Gate to Drain Charge (Note 7)	Q_{GD}			3.6		
Gate Charge at Threshold (Note 7)	$Q_{G(TH)}$			4.3		
Output Charge (Note 6)	Q_{OSS}	V_{DS} = 20 V, V_{GS} = 0 V		34		
Source to Drain Recovery Charge (Note 6)	Q_{RR}			0		

All measurements were done with substrate connected to source.

Radiation Characteristics

EPC Space eGaN® HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON | V_{GS} = 5 V
NO BIAS | V_{DS} = V_{GS} = 0 V
OFF | V_{DS} = 80% B_{VDSS}

Electrical Characteristics up to 1000 krads *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	V_{GS} = 0 V	40			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 20 mA	0.8	1.3	2.5	
Drain to Source Leakage	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		0.2	0.5	mA
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 6 V		0.085	4	
Gate to Source Reverse Leakage		V_{GS} = -4 V		0.3	1	
Drain to Source Resistance	$R_{DS(on)}$	I_D = 20 A, V_{GS} = 5 V		0.5	0.6	mΩ

Typical Single Event Effect Safe Operating Area

Note : All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.

Test	Environment				V_{DS} Voltage (V)	
See SOA	Ion	LET MeV/(mg/cm²) in Si (+/-5%)	Range mm (+/- 7.5%)	Energy MeV (+/-10%)	V_{GS} = 0 V	V_{GS} = -4V
	Bi	80	2.55	127	40	40

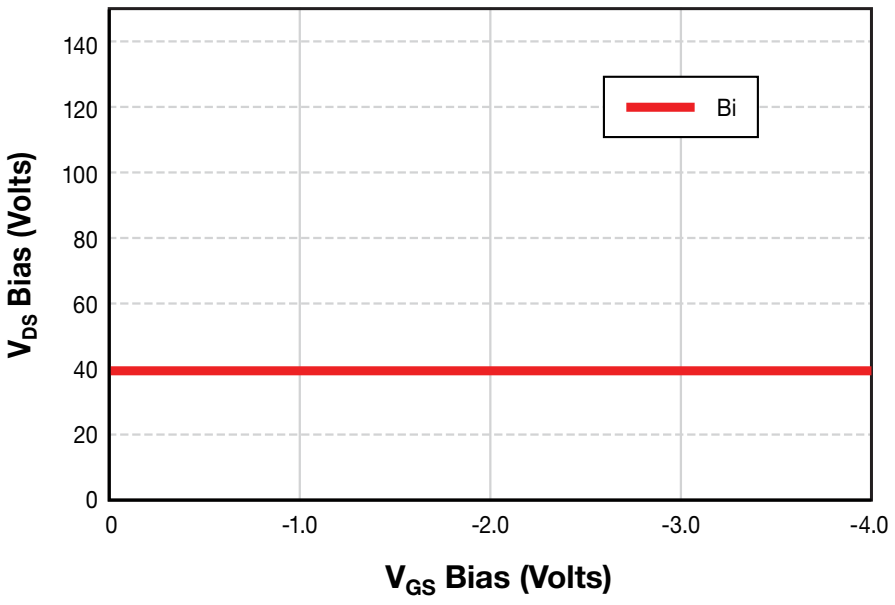


Figure 1: Typical Single Event Effect Safe Operating Area

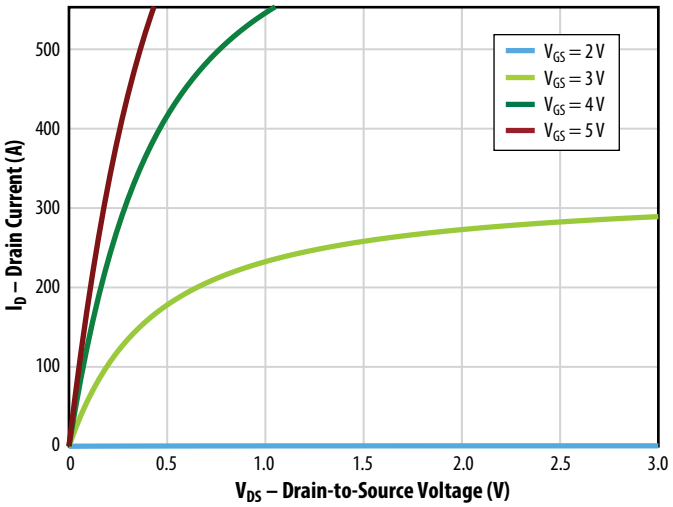


Figure 2: Typical Output Characteristics at 25°C

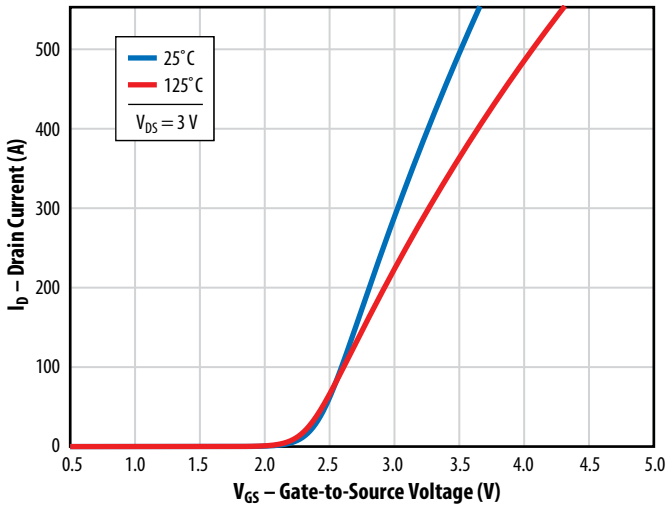


Figure 3: Typical Transfer Characteristics

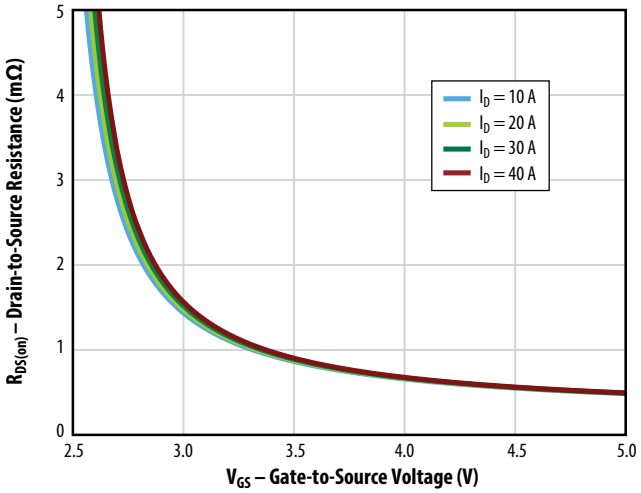


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

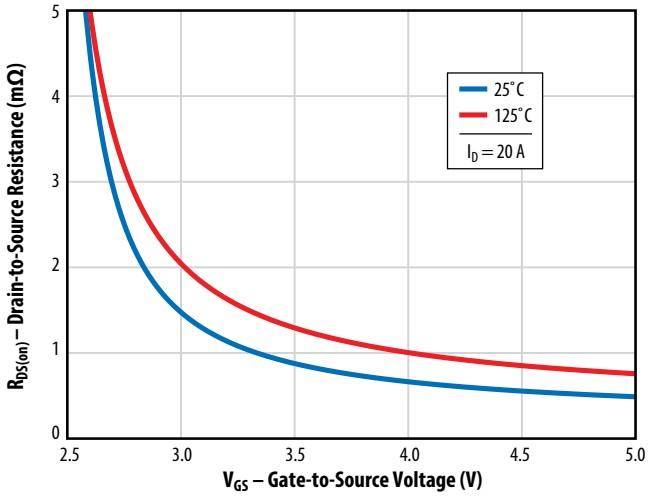


Figure 5: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

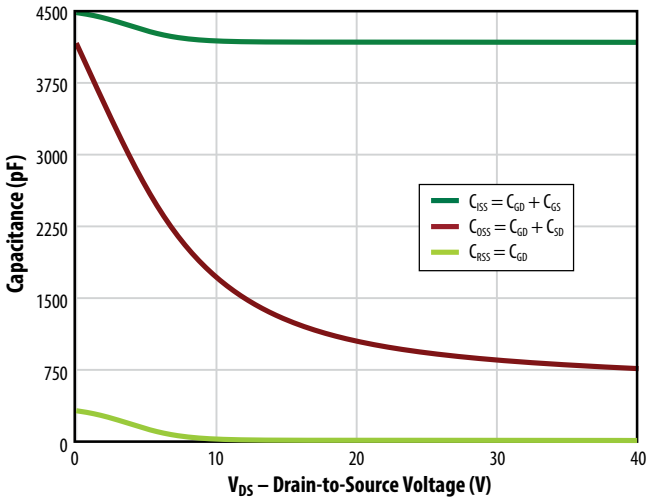


Figure 6: Typical Capacitance (Linear Scale)

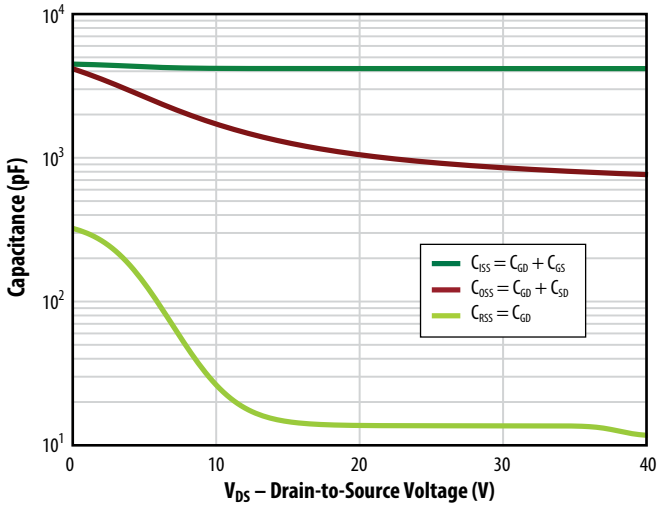


Figure 7: Typical Capacitance (Log Scale)

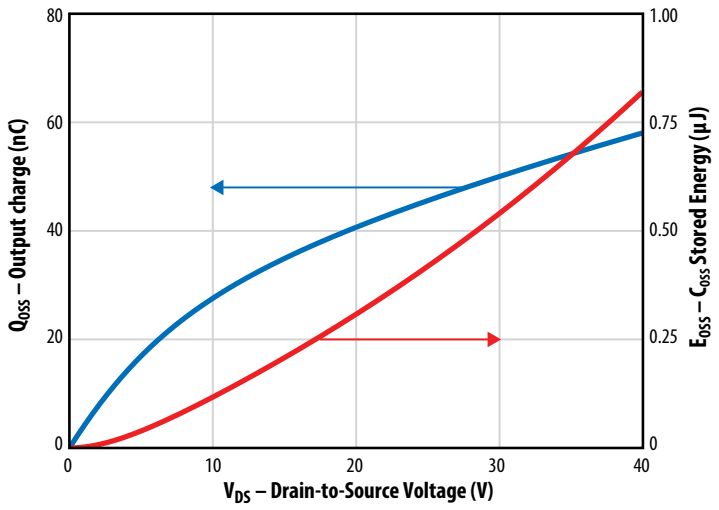


Figure 8: Typical Output Charge and C_{OSS} Stored Energy

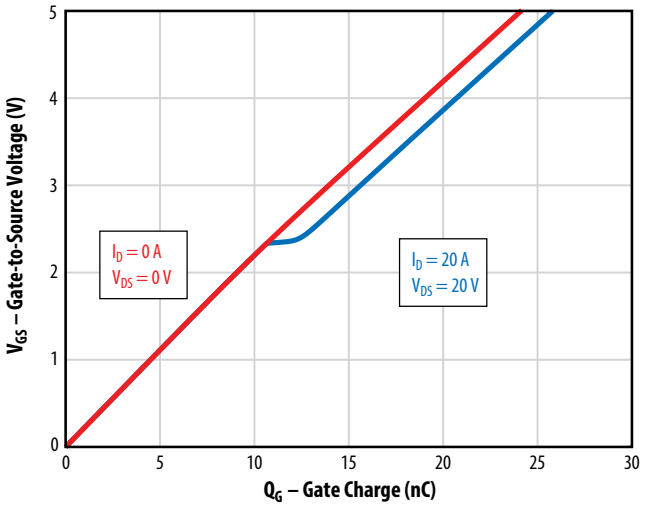


Figure 9: Typical Gate Charge

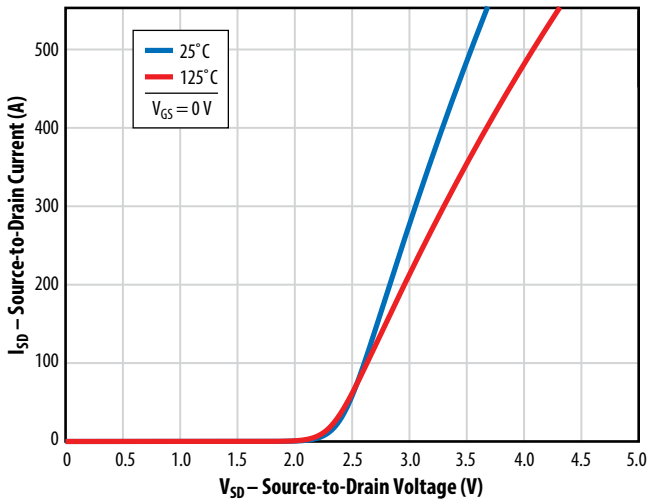


Figure 10: Typical Reverse Drain-Source Characteristics

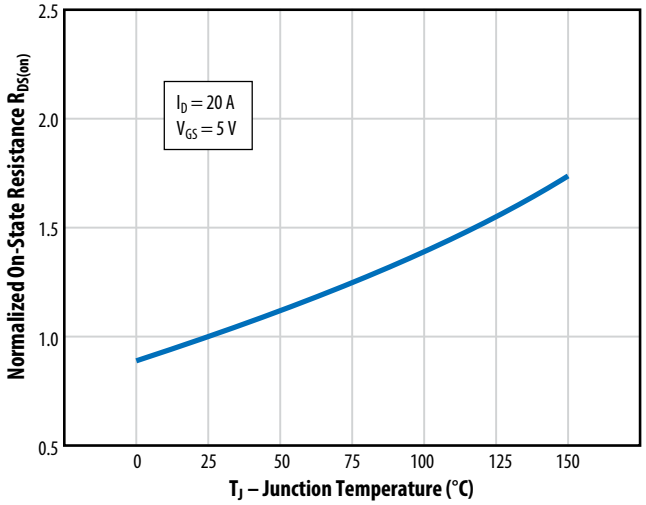


Figure 11: Typical Normalized On-State Resistance vs. Temperature

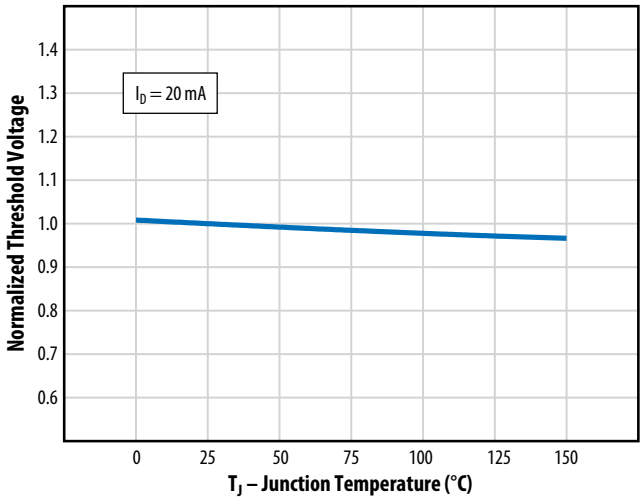


Figure 12: Typical Normalized Threshold Voltage vs. Temperature

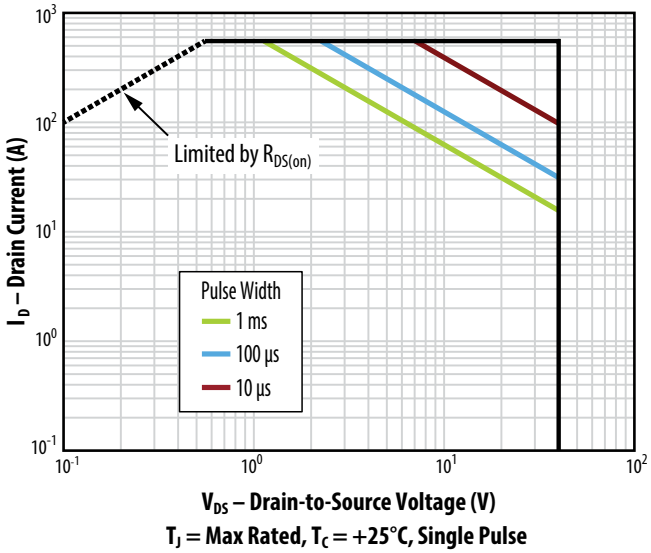


Figure 13: Safe Operating Area

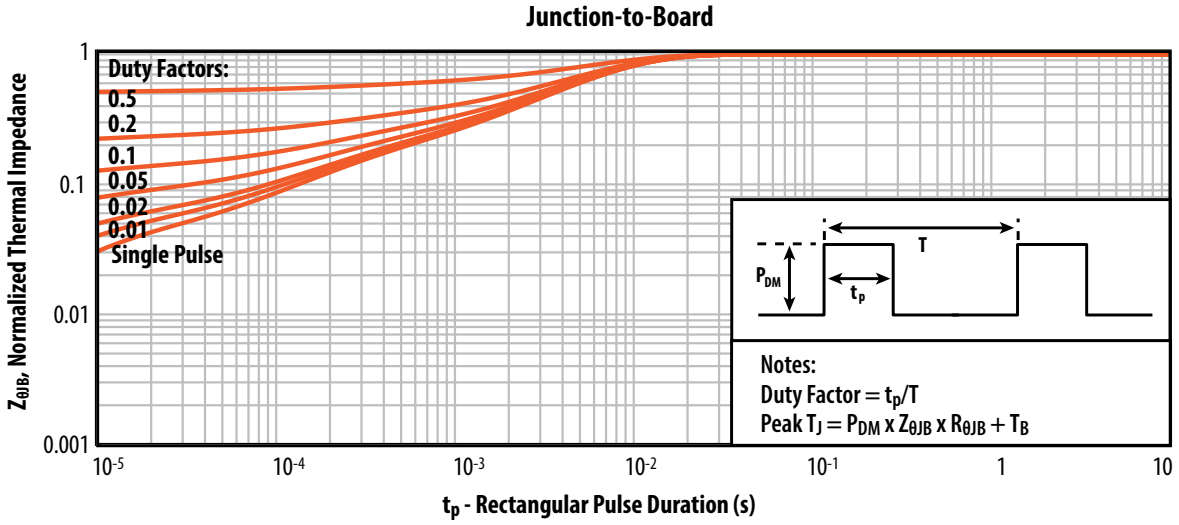


Figure 14: Typical Transient Thermal Response Curves

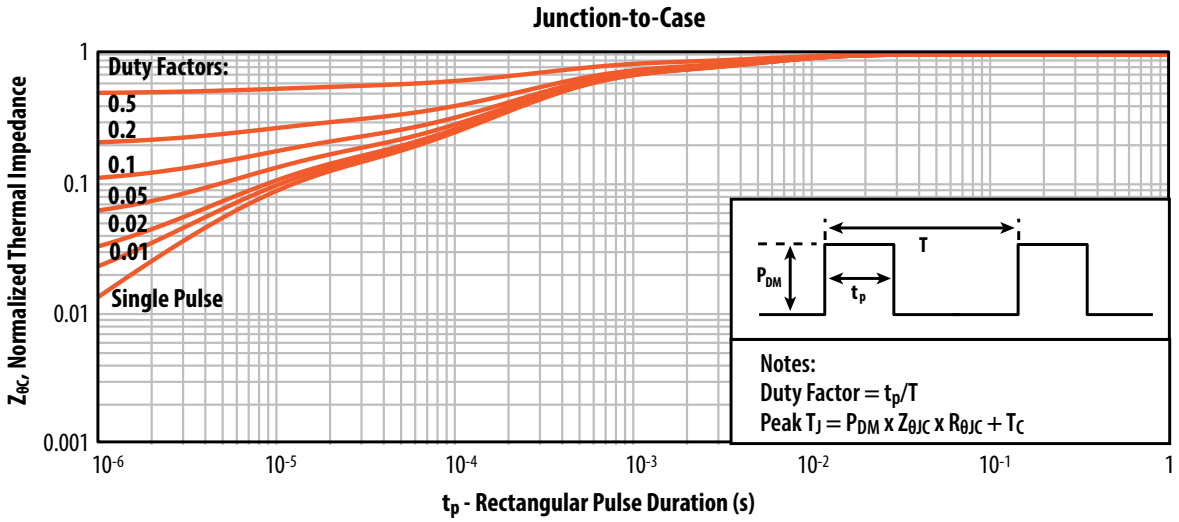
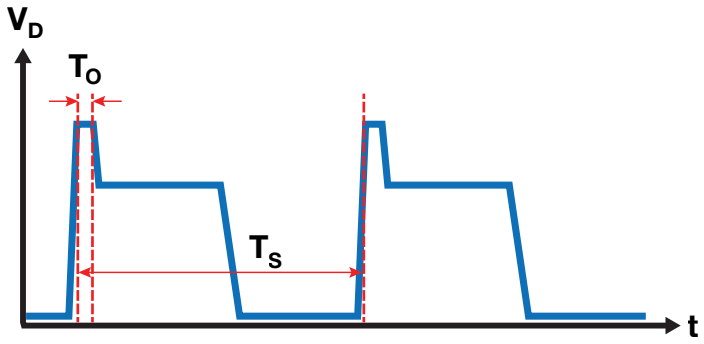


Figure 15: Typical Transient Thermal Response Curves



1% is the ratio between T_O (overvoltage duration) and T_S (one switching period).

Figure 16: Duty Cycle Factor (DC_{Factor}) Illustration for Repetitive Overvoltage Specification

Typical Thermal Concept

The EPC7065PCSH can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

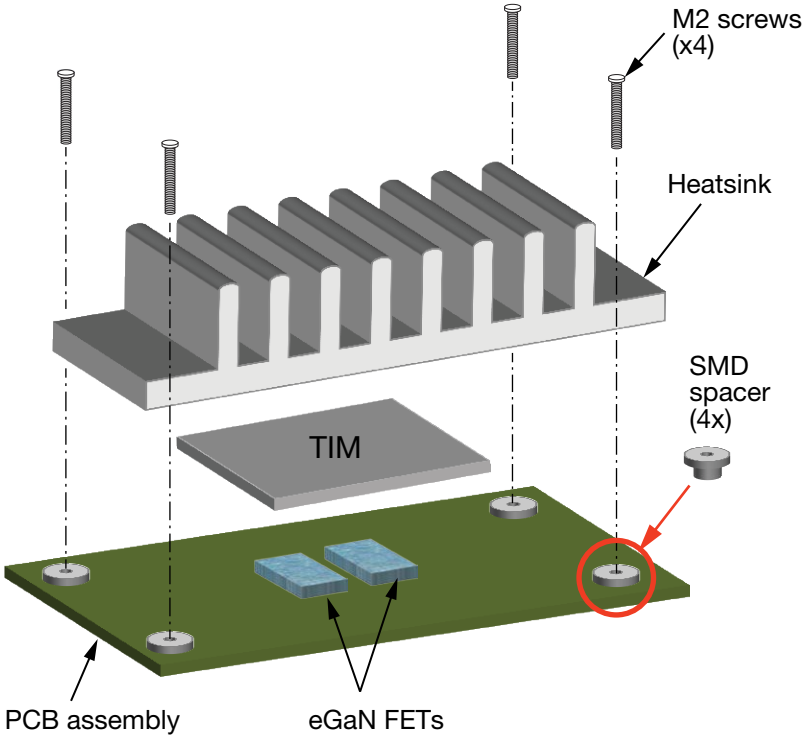


Figure 17: Exploded view of heatsink assembly using screws

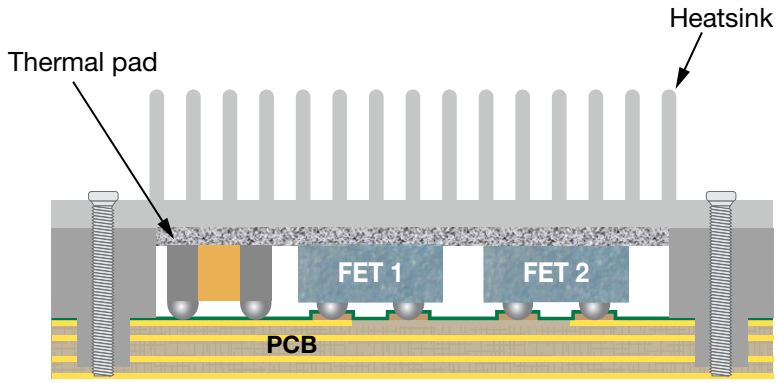
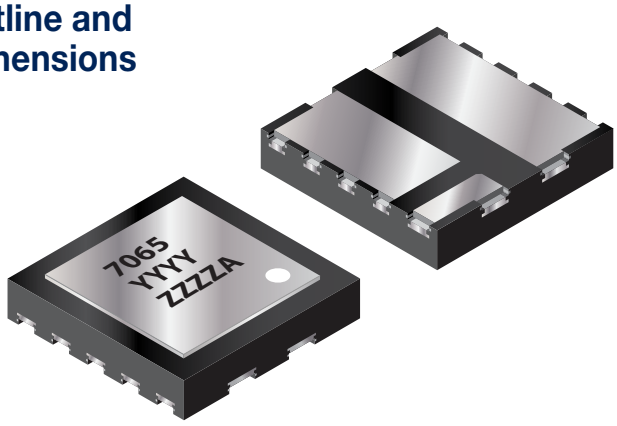


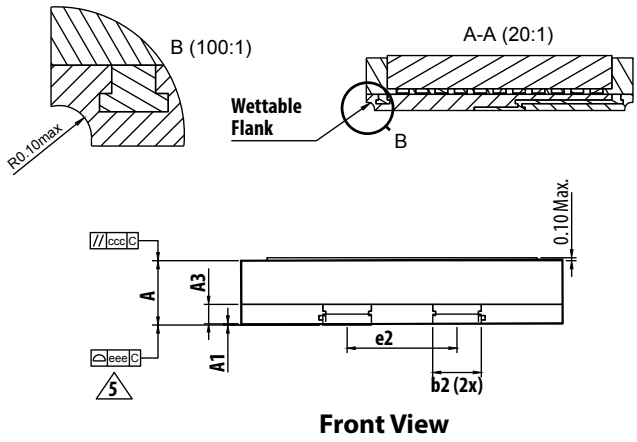
Figure 18: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

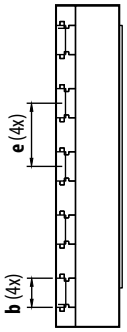
The thermal design can be optimized by using the **GaN FET Thermal Calculator** on EPC's website.

Package Outline and Dimensions

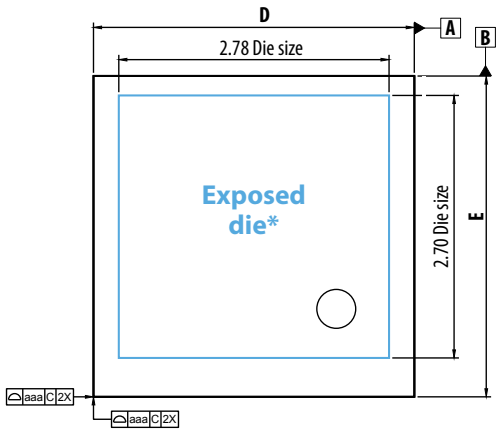


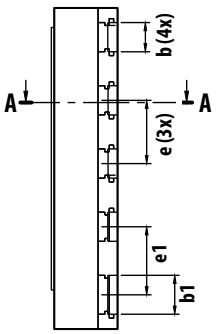


Side View

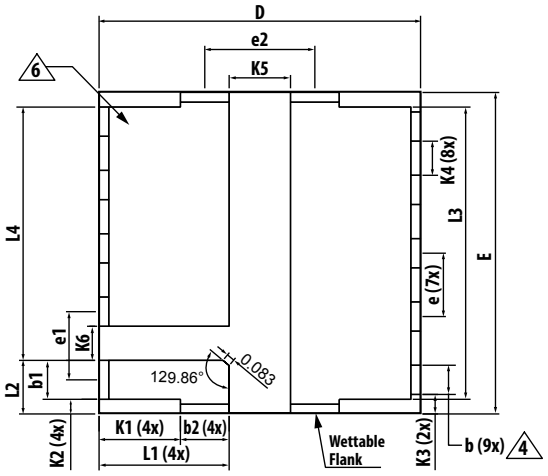


Top View





Bottom View



*The exposed die is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

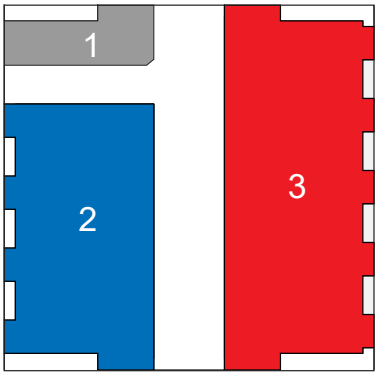
Symbol	Dimension (mm)			Note
	MIN	NOM	MAX	
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.25	0.30	0.35	4
b1	0.35	0.40	0.45	4
b2	0.45	0.50	0.55	4
D	3.20	3.30	3.40	
E	3.20	3.30	3.40	
e	0.65			BSC
e1	0.7			BSC
e2	1.13			BSC
L1	1.235	1.335	1.435	
L2	0.45	0.55	0,65	
L3	2.9	3	3.1	
L4	2.15	2.25	2.35	

Symbol	Dimension (mm)			Note
	MIN	NOM	MAX	
K1	0.835			REF
K2	0.15			REF
K3	0.2			REF
K4	0.35			REF
K5	0.63			REF
K6	0.35			REF
aaa	0.05			
ccc	0.1			
eee	0.08			
N	3			3

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension **b** applies to the metalized terminal and a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.
6. Lead plating is NiPdAu (1.5/0.01/0.005 µm min.) Au as the finish.

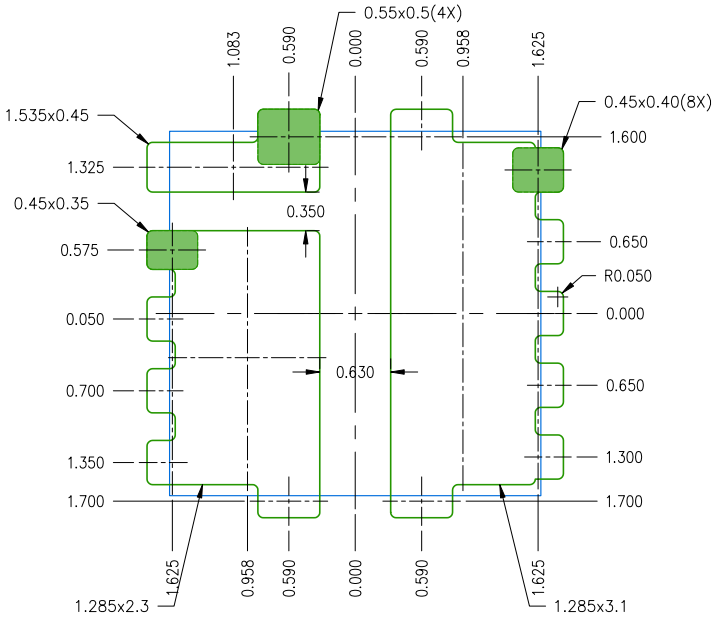
TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain

RECOMMENDED SOLDER MASK PATTERN

(units in mm)



Legend:

Part Outline

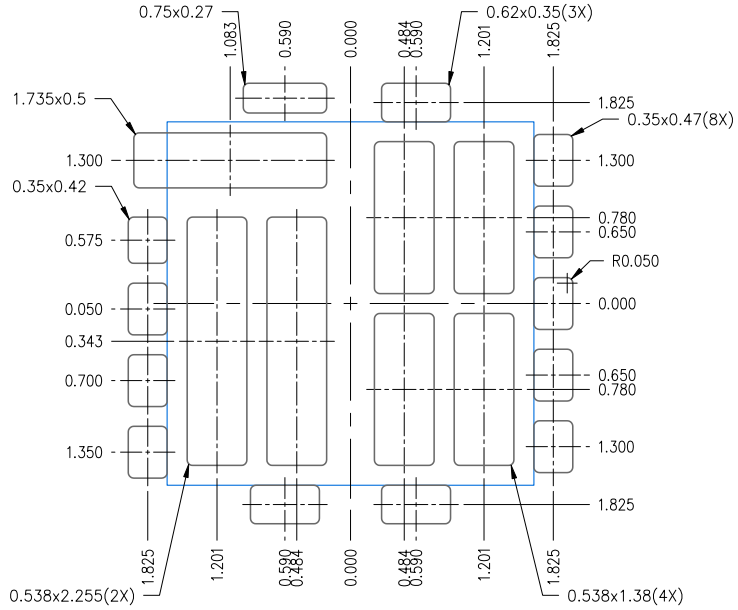
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



Legend:

Part Outline

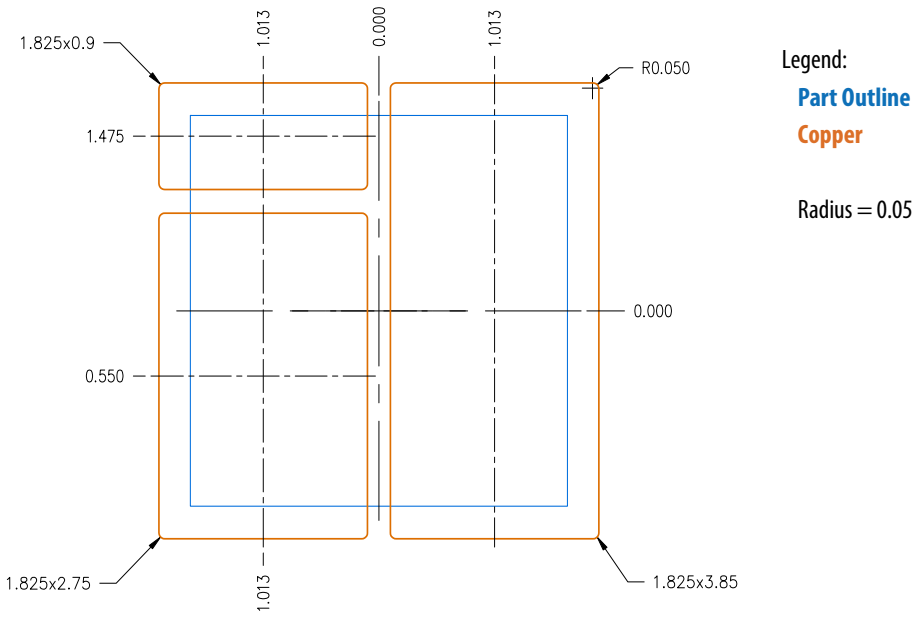
Stencil Opening

The recommended stencil should be 4mils (100 µm) thick, must be laser cut, and have openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.

RECOMMENDED COPPER DRAWING

(units in mm)



Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.

Note 3. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 4. $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 5. $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 6. Guaranteed by design/device construction. Not Tested.

Note 7. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on})is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off}/t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

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Patents

EPC Corporation and EPC Space hold numerous worldwide patents. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with local patent laws.

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Information subject to change without notice.

Status	Version	Date	Remark
1.0	Preliminary	30 March 2026	Preliminary Release