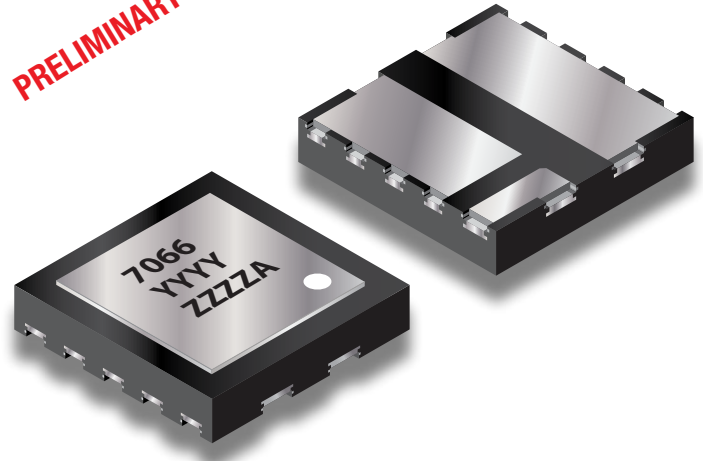


## Features

- Moisture Rating MSL1
- 3.3 x 3.3 mm QFN package
- Ultra-low  $Q_G$  for High Frequency
- PQFN Package with Backside Thermal Pad
- No reverse recovery



PRELIMINARY



**EPC7066PC**  
eGaN<sup>®</sup> FET in a  
Plastic Surface Mount  
25 V, 101 A, 0.37 mΩ

## Applications

- High Performance, high power-density DC-DC Conversion
- High-Frequency DC-DC Converters
- Synchronous Rectifiers
- Point of Load Buck Converter

## Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	0.9	

## Description

EPC's eGaN<sup>®</sup> power switching transistors have been specifically designed for critical applications in DC-DC conversion. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low  $R_{DS(on)}$  values. The lateral structure of the die provides for very low gate charge ( $Q_G$ ) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging. EPC7066PC has been specifically designed for synchronous rectifier applications on the secondary side of a 48 V–8 or 5 V LLC converter, where it brings an industry leading low  $R_{DS(on)} \times Q_G$  figure of merit and enables higher frequency and higher efficiency operation. EPC7066PC is also for point of load buck converters.

## Maximum Rating

Symbol	Parameter-Conditions	Value	Units
$V_{DS}$	Drain-to-Source Voltage (Note 1)	25	V
$V_{DS(tr)}$	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	30	
$I_D$	Continuous Drain Current at $V_{GS} = 5 V$	101	A
	Pulsed (25°C, $T_{PULSE} = 300 \mu s$ )	699	
$V_{GS}$	Gate-to-Source Voltage	+6 / -4	V
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

(1) Pulsed repetitively, duty cycle factor ( $DC_{Factor}$ )  $\leq 1\%$ ;  
See Figure 13 and **Reliability Report Phase 16**, Section 3.2.6

Static Characteristics# ( $T_J = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	$B_{VDSS}$	$V_{GS} = 0 V, I_D = TBD$	25			V
Drain to Source Leakage	$I_{DSS}$	$V_{GS} = 0 V, V_{DS} = 25 V$		0.1		mA
		$V_{GS} = 0, V_{DS} = 25 V, T_J = 125^\circ C$			1	
Gate to Source Forward Leakage	$I_{GSS}$	$V_{GS} = 5 V$		0.1		mA
Gate to Source Forward Leakage		$V_{GS} = 5 V, T_J = 125^\circ C$		0.5		
Gate to Source Reverse Leakage		$V_{GS} = -2 V$		0.3		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 24 mA$	0.8	1.4	2.5	V
Drain to Source On Resistance (Note 3)	$R_{DS(on)}$	$V_{GS} = 5 V, I_D = 20 A$		0.37		m $\Omega$
Source to Drain Forward Voltage	$V_{SD}$	$I_S = 0.5 A, V_{GS} = 0 V$		1.6		V

Dynamic Characteristics# ( $T_J = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	$C_{ISS}$	$V_{DS} = 12 V, V_{GS} = 0 V$		5984		pF
Reverse Transfer Capacitance	$C_{RSS}$			47		
Output Capacitance	$C_{OSS}$			1320		
Effective Output Capacitance, Energy Related	$C_{OSS(ER)}$	$V_{GS} = 0 V, V_{DS} = 0$ to 12 V		1763		
Effective Output Capacitance, Time Related	$C_{OSS(TR)}$			2141		
Total Gate Charge (Note 6)	$Q_G$	$V_{DS} = 12 V, V_{GS} = 5 V, I_D = 20 A$		34		nC
Total Gate Charge Synchronous (Note 6)	$Q_{G SYNC}$	$V_{DS} = 0 V, V_{GS} = 5 V, I_D = 0 A$		32		
Gate to Source Charge (Note 7)	$Q_{GS}$	$V_{DS} = 12 V, I_D = 20 A$		12		
Gate to Drain Charge (Note 7)	$Q_{GD}$			1.5		
Output Charge (Note 6)	$Q_{OSS}$	$V_{DS} = 12 V, V_{GS} = 0 V$		26		
Source to Drain Recovery Charge (Note 6)	$Q_{RR}$			0		

All measurements were done with substrate connected to source.

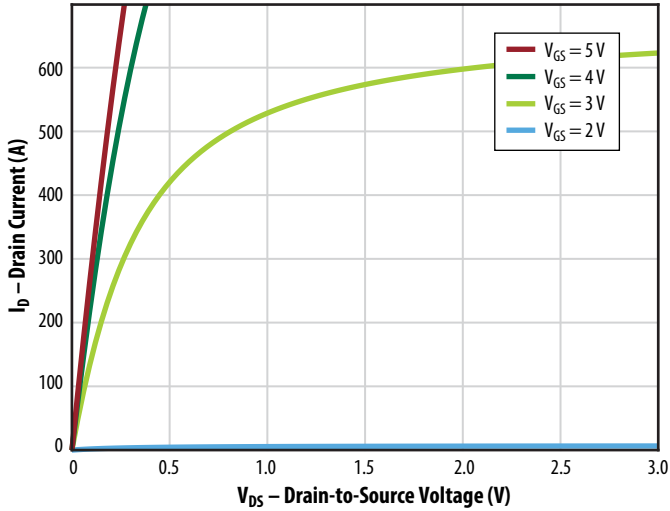


Figure 1: Typical Output Characteristics at 25°C

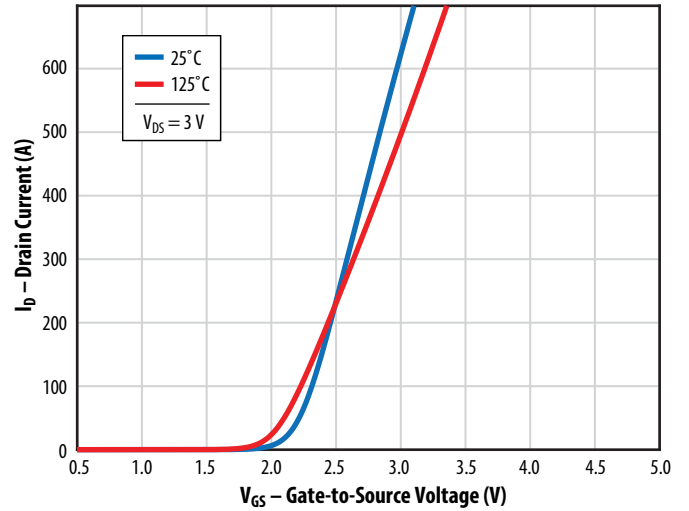


Figure 2: Typical Transfer Characteristics

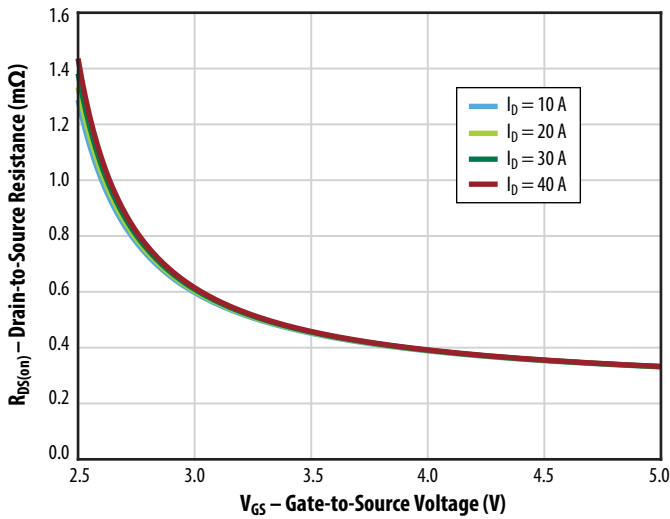


Figure 3: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

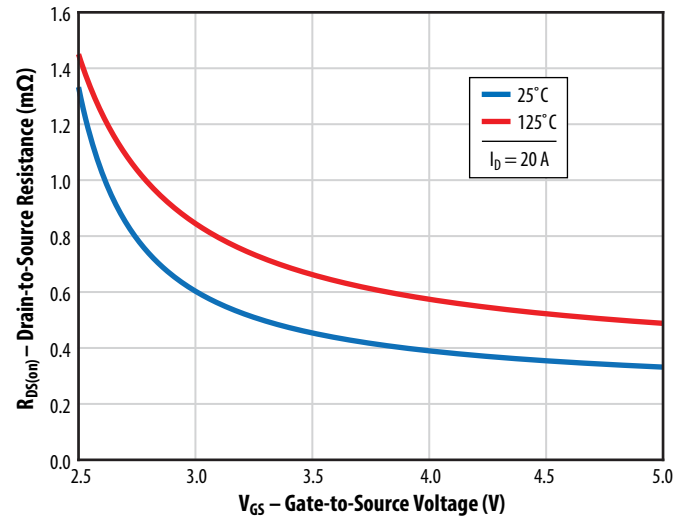


Figure 4: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

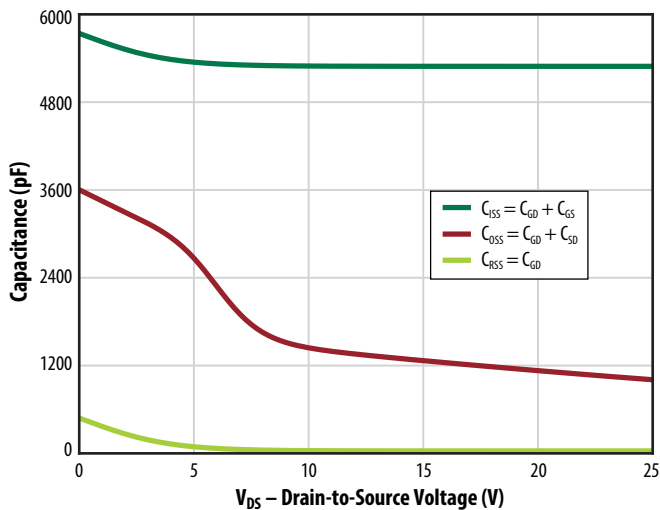


Figure 5a: Typical Capacitance (Linear Scale)

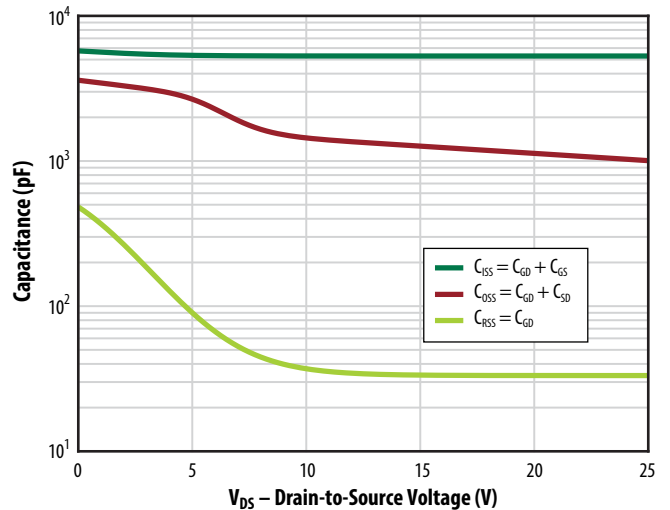


Figure 5b: Typical Capacitance (Log Scale)

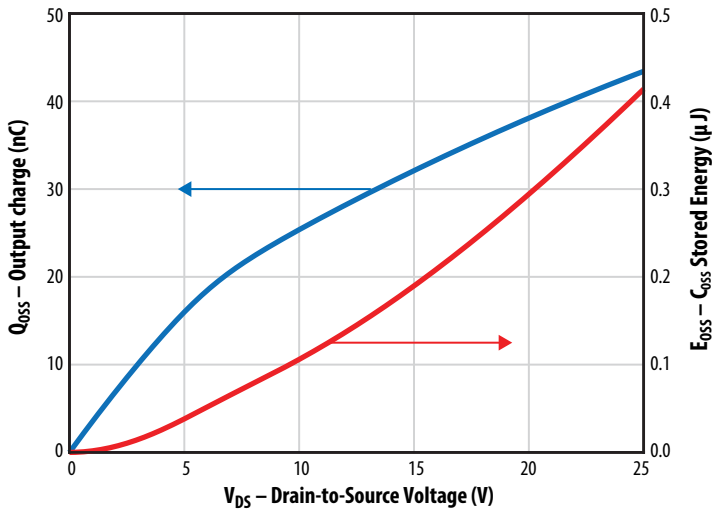


Figure 6: Typical Output Charge and  $C_{OSS}$  Stored Energy

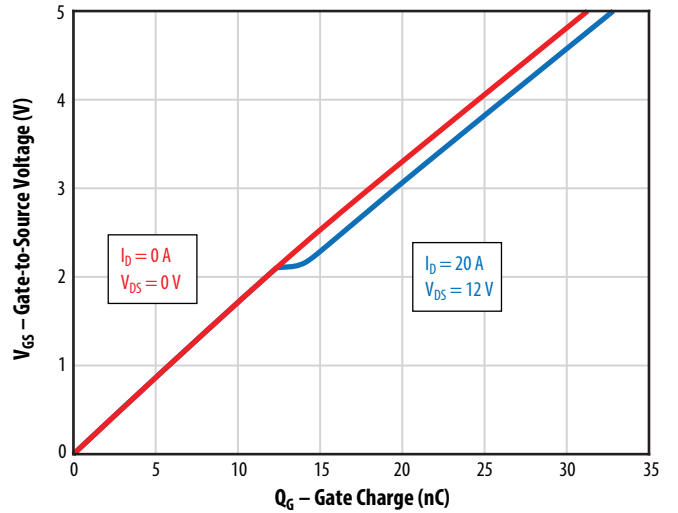
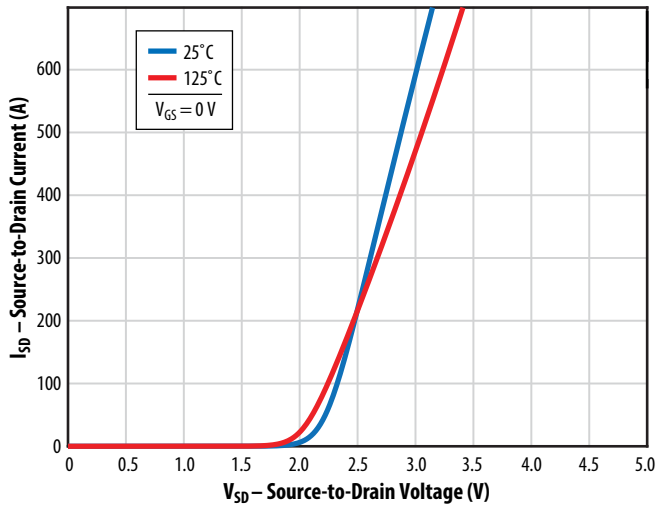


Figure 7: Typical Gate Charge



Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0V for OFF

Figure 8: Typical Reverse Drain-Source Characteristics

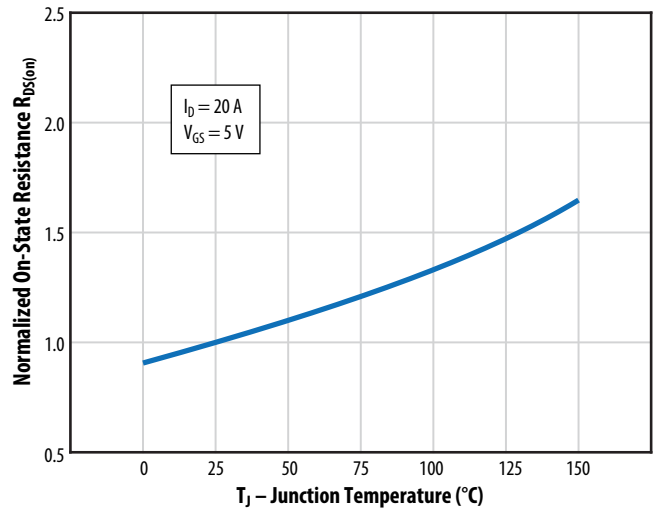


Figure 9: Typical Normalized On-State Resistance vs. Temperature

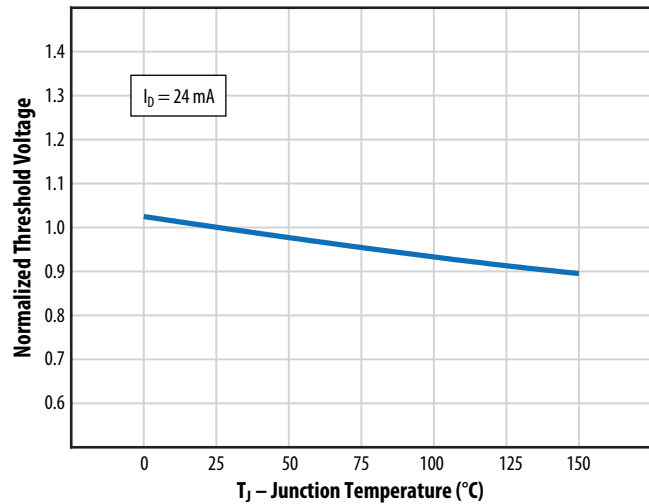


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

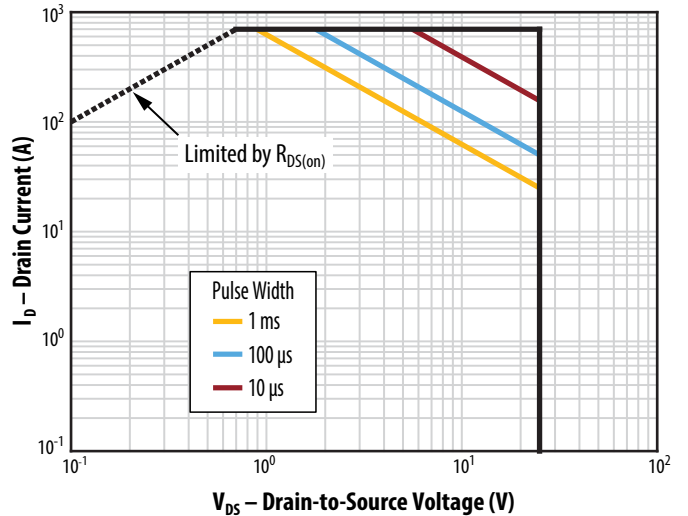


Figure 11: Safe Operating Area

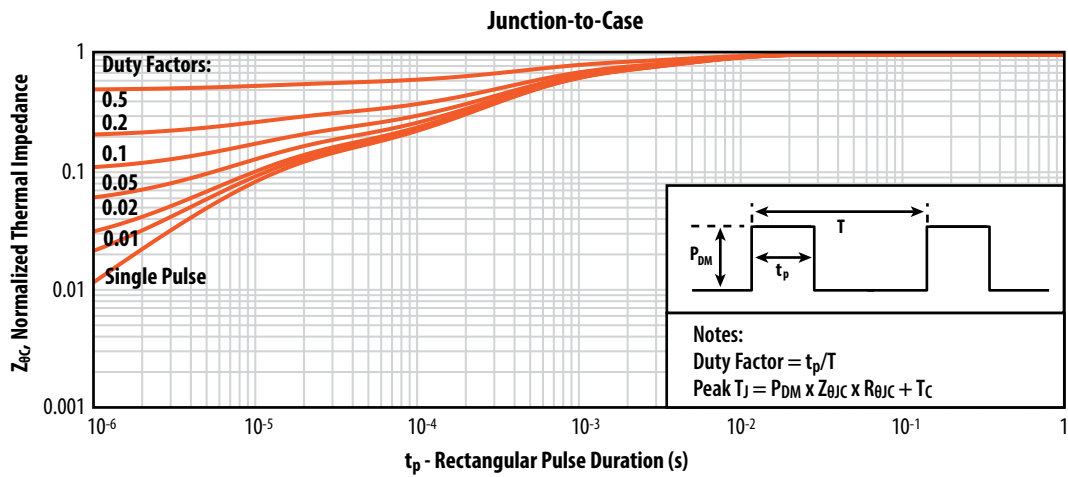
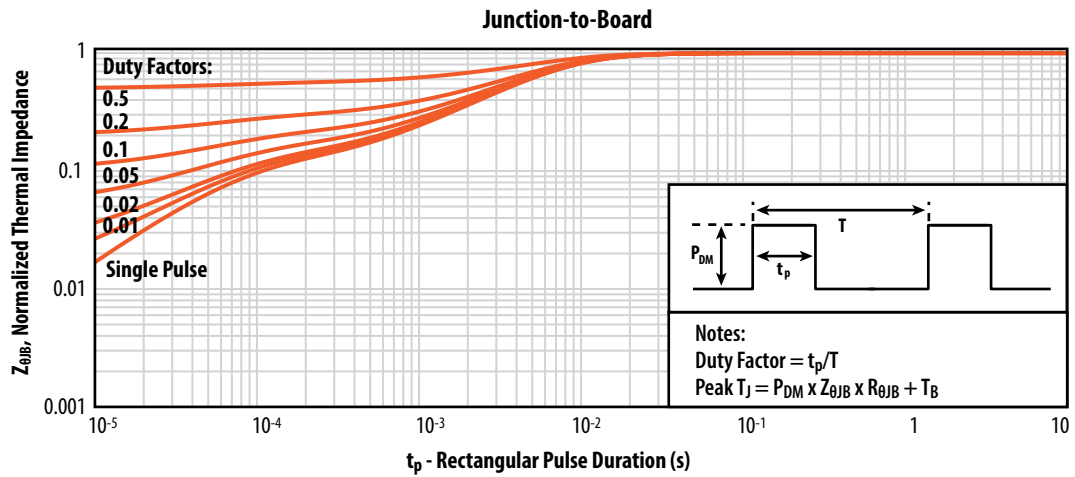


Figure 12: Typical Transient Thermal Response Curves

## Typical Thermal Concept

The EPC7066PC can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. **Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.**

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

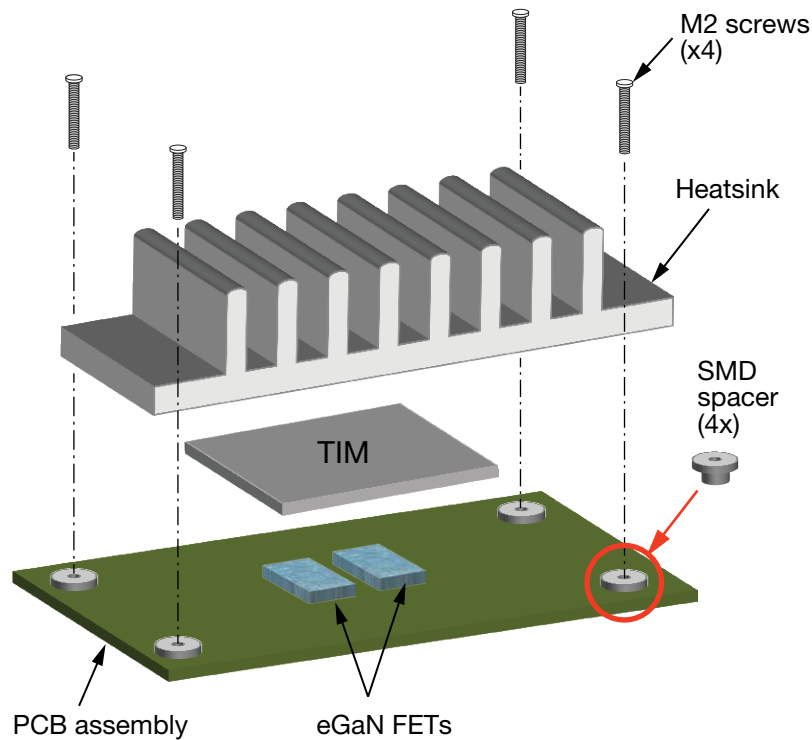


Figure 18: Exploded view of heatsink assembly using screws

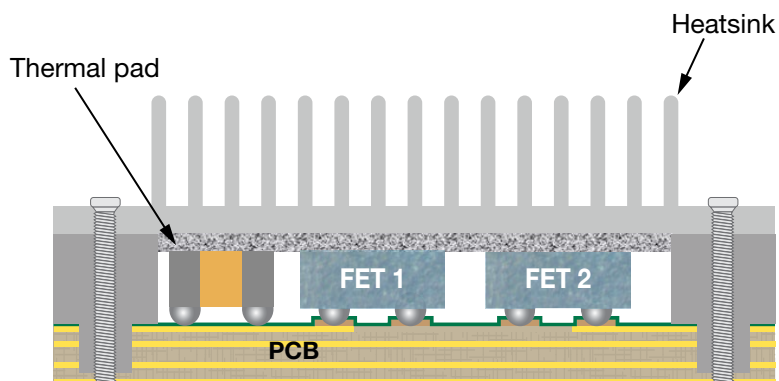


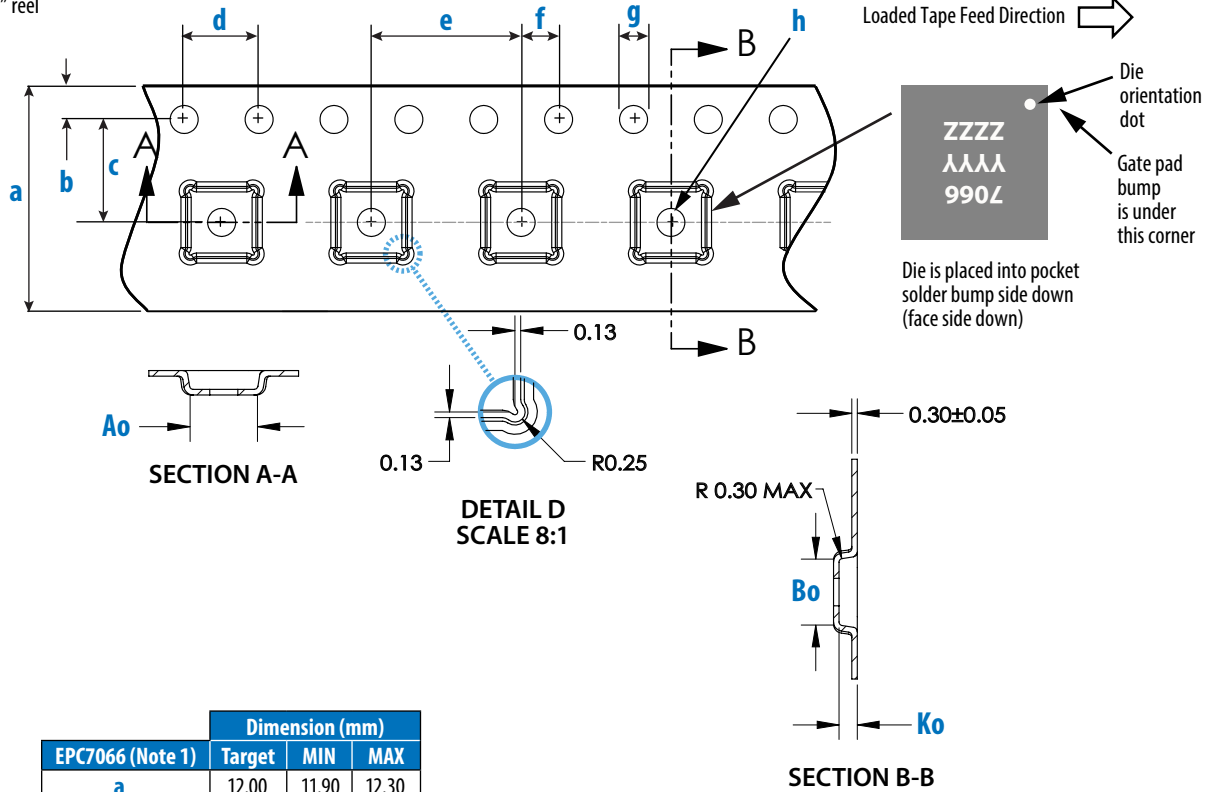
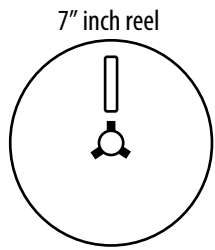
Figure 19: A cross-section image of dual sided thermal solution

**Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI**

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

**TAPE AND REEL CONFIGURATION**

8 mm pitch, 12 mm wide tape on 7" reel

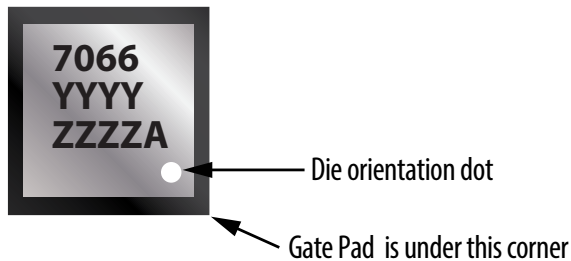


EPC7066 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
<b>a</b>	12.00	11.90	12.30
<b>b</b>	1.75	1.65	1.85
<b>c</b> (Note 2)	5.50	5.45	5.55
<b>d</b>	4.00	3.90	4.10
<b>e</b>	8.00	7.90	8.10
<b>f</b> (Note 2)	2.00	1.95	2.05
<b>g</b>	1.50	1.50	1.60
<b>h</b>	1.50	1.50	1.60
<b>Ao</b>	3.6	3.4	3.5
<b>Bo</b>	3.6	3.4	3.5
<b>Ko</b>	1.0	0.9	1.1

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

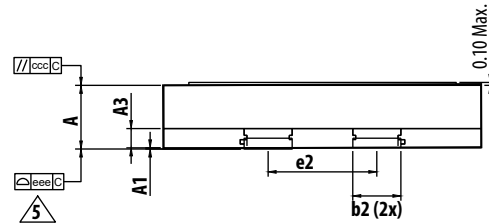
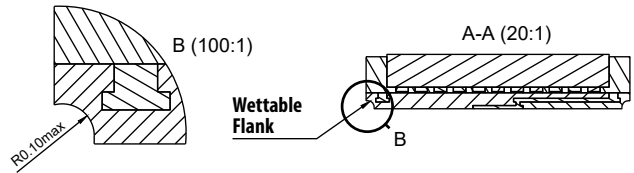
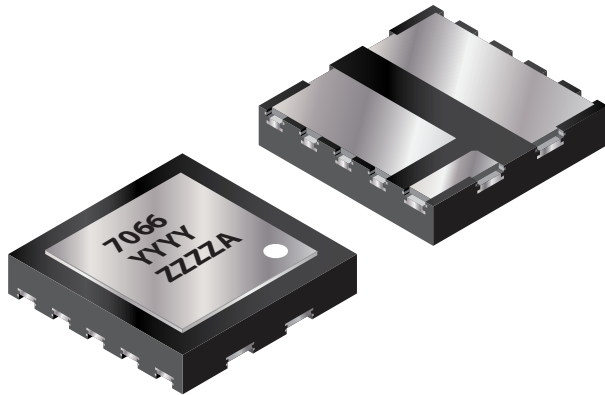
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

**Part Marking**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC7066PC	7066	YYYY	ZZZZA

## PACKAGE OUTLINE AND DIMENSIONS

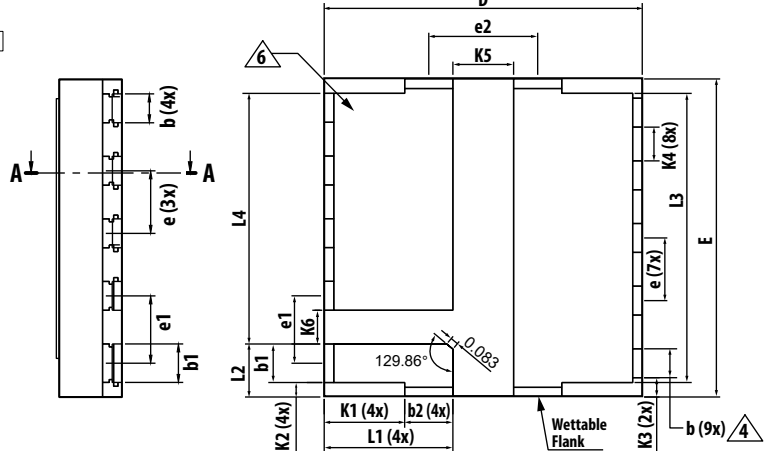
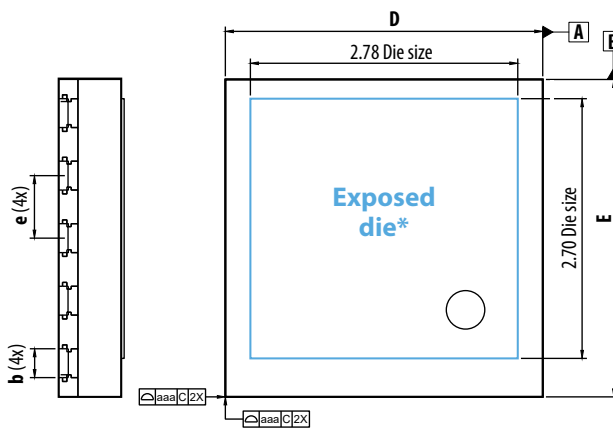


Front View

Side View

Top View

Bottom View



\*The exposed die is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

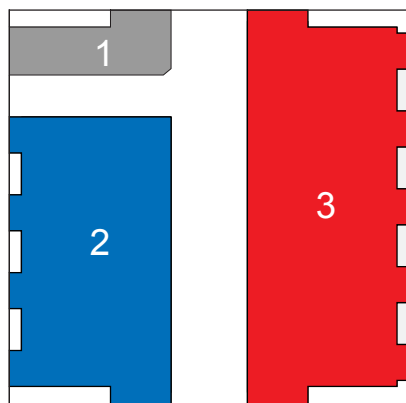
SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.25	0.30	0.35	4
b1	0.35	0.40	0.45	4
b2	0.45	0.50	0.55	4
D	3.20	3.30	3.40	
E	3.20	3.30	3.40	
e		0.65		BSC
e1		0.70		BSC
e2		1.13		BSC
L1	1.235	1.335	1.435	
L2	0.45	0.55	0.65	
L3	2.90	3.00	3.10	
L4	2.15	2.25	2.35	

SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
K1		0.835		REF
K2		0.15		REF
K3		0.20		REF
K4		0.35		REF
K5		0.63		REF
K6		0.35		REF
aaa		0.05		
ccc		0.10		
eee		0.08		
N		3		3

### Notes:

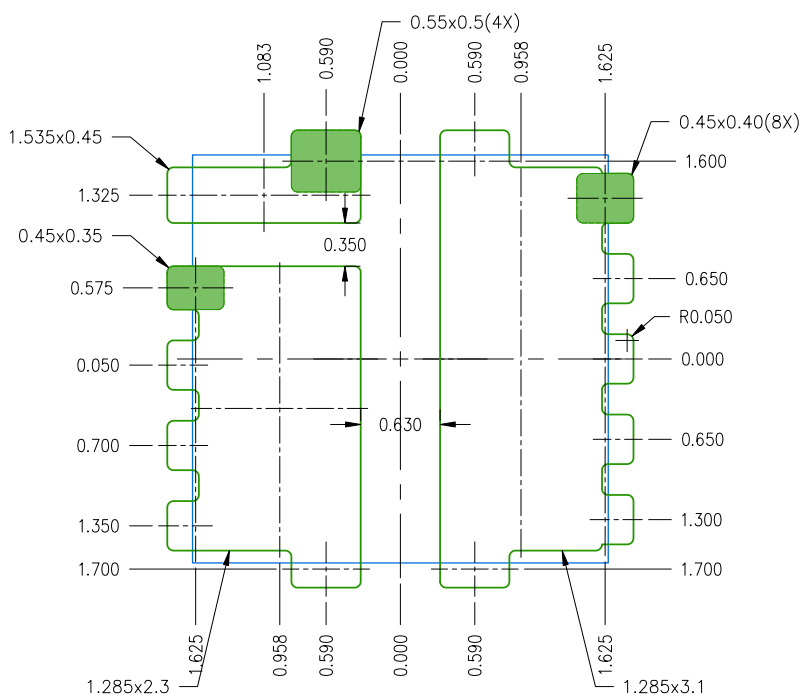
- Dimensioning and tolerancing conform to ASME Y14.5-2009
- All dimensions are in millimeters
- N is the total number of terminals
- Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
- Coplanarity applies to the terminals and all the other bottom surface metallization.
- Lead plating is NiPdAu (1.5/0.01/0.005 μm min). Au as the finish.

TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain

RECOMMENDED LAND PATTERN  
(units in mm)



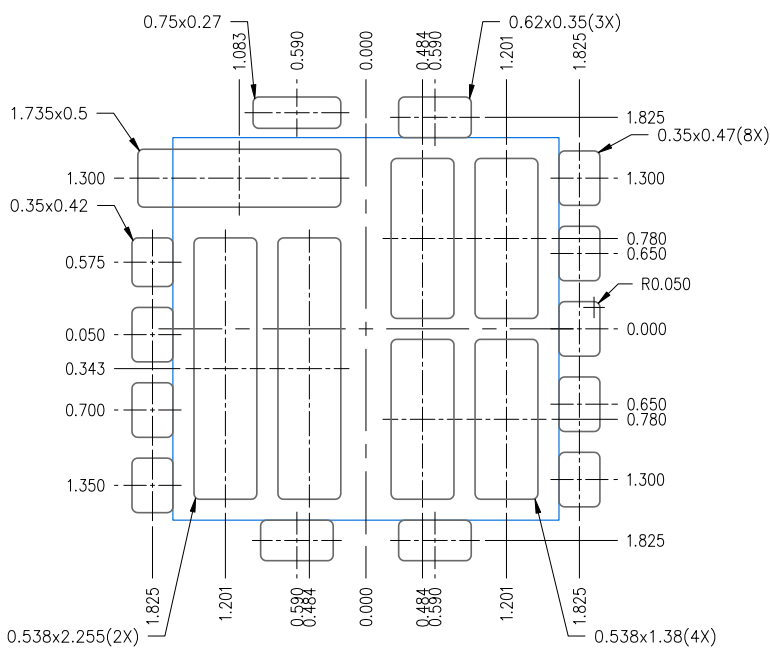
Legend:

Part Outline  
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING  
(units in mm)



Legend:

Part Outline  
Stencil Opening

The recommended stencil should be 4mils (100 μm) thick, must be laser cut, and have openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.



- Note 1. Never exceed the absolute maximum  $V_{DS}$  of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum  $V_{GS}$  of the device otherwise permanent damage/destruction may result. We recommend a  $V_{GS}$  of 5 V for optimum operation across life and radiation.
- Note 3. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80  $\mu$ s and duty cycle is 1%, maximum.
- Note 4.  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .
- Note 5.  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .
- Note 6. Guaranteed by design/device construction. Not Tested.
- Note 7. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current ( $I_{const}$ ) is provided to the Gate of the DUT during the time that the ground switch ( $G_S$ ) is OFF ( $t_{off}$ ). The DUT is switched ON and OFF using ground-sensed switch  $G_S$ . The gate current is adjusted to yield the desired charge per unit time ( $I_{const} \cdot \text{time per division}$ ) on the measuring oscilloscope. The  $G_S$  pulse drive ON time ( $t_{on}$ ) is adjusted for the desired observability of the gate-source voltage ( $V_{GS}$ ) waveform. The maximum duty cycle of the ground switch ( $t_{off}/t_{on}$ ) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5  $V_{DC}$ .

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Information subject to change without notice.

Change Log

Status	Version	Date	Remark
1.0	Preliminary datasheet	27 April 2026	Production Release