Features

- 100 V
- Low $R_{DS(on)}$
- 3 x 5 mm QFN package
- Exposed top for top-side thermal management
- Moisture rating MSL1
- Enhanced thermal-max package

Applications

- Satellite and avionics
- Deep space probes
- High speed DC-DC conversion
- Motor controllers

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint
- Excellent thermal

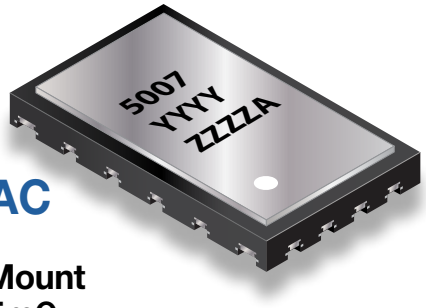
Application Notes

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.5	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to- Ambient (using JEDEC 51-2 PCB)	44	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to- Ambient (using EPC90156 EVB)	25	

PRELIMINARY



EPCS5007PAC

eGaN® FET in a Plastic Surface Mount 100 V, 133 A, 0.75mΩ

Description

The EPCS5007PAC is a plastic QFN device with an exposed top for excellent thermal management. It is tailored to high frequency DC-DC motor drive applications.

The thermal resistance to case top is ~0.2 °C/W, resulting in excellent thermal behavior and easy cooling. The device features an enhanced PQFN "Thermal-Max" package. The exposed top enhances top-side thermal management and the side-wettable flanks guarantee that the complete side-pad surface is wetted with solder during the reflow soldering process, which protects the copper and allows soldering to occur on this external flank area for easy optical inspection.

Compared to a Si MOSFET, the footprint of 15 mm^2 is less than half of the size of the best-in-class Si MOSFET with similar $R_{DS(on)}$ and voltage rating, Q_G and Q_{GD} are significantly smaller and Q_{RR} is 0. This results in lower switching losses and lower gate driver losses. Moreover, EPCS5007PAC is very fast and can operate with deadtime less than 10 ns for higher efficiency and Q_{RR} = 0 is a big advantage for reliability and EMI. In summary, EPCS5007PAC allows the highest power density due to enhanced efficiency, smaller size, and higher switching frequency for smaller inductor and fewer capacitors.

The EPCS5007PAC enables designers to improve efficiency and save space. The excellent thermal behavior enables easier and lower cost cooling. The ultra-low capacitance and zero reverse recovery of the eGaN® FET enables efficient operation in many topologies. Performance is further enhanced due to the small, low inductance footprint.

Maximum Rating

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain-to-Source Voltage (Note 1)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (Repetitive Transient)(1)	120	
I_D	Continuous ($T_J \leq 125°C$)	133	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	697	
V_{GS}	Gate-to-Source Voltage (Note 2)	+6 / -4	V
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–55 to 175	

(1) Pulsed repetitively, duty cycle factor (DC_{Factor}) ≤ 1%;
See Figure 13 and **Reliability Report Phase 16**, Section 3.2.6

Static Characteristics *(T_J = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 0.5 mA	100			V
Drain to Source Leakage	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V		0.01	0.15	mA
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 5 V		0.05	4	
Gate to Source Forward Leakage		V_{GS} = 5 V, T_J = 125°C		0.15	9	
Gate to Source Reverse Leakage		V_{GS} = -4 V		0.002	0.2	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 15 mA	0.8	1.1	2.5	V
Drain to Source On Resistance (Note 3)	$R_{DS(on)}$	V_{GS} = 5 V, I_D = 50 A		0.75	1	mΩ
Source to Drain Forward Voltage	V_{SD}	I_S = 0.5 A, V_{GS} = 0 V		1.6	3	V

Dynamic Characteristics# *(T_J = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 50 V, V_{GS} = 0 V		3599	4373	pF
Reverse Transfer Capacitance	C_{RSS}			13		
Output Capacitance	C_{OSS}			1019	1284	
Effective Output Capacitance, Energy Related (Note 4)	$C_{OSS(ER)}$	V_{DS} = 0 to 50 V, V_{GS} = 0 V		1419		
Effective Output Capacitance, Time Related (Note 5)	$C_{OSS(TR)}$			1796		
Gate Resistance (Note 6)	R_G			0.4		Ω
Total Gate Charge (Note 6)	Q_G	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 50 A		28	34	nC
Gate to Source Charge (Note 7)	Q_{GS}	V_{DS} = 50 V, I_D = 50 A		8.5		
Gate to Drain Charge (Note 7)	Q_{GD}			3.8		
Gate Charge at Threshold (Note 7)	$Q_{G(TH)}$			6		
Output Charge (Note 6)	Q_{OSS}	V_{DS} = 50 V, V_{GS} = 0 V		90	112	
Source to Drain Recovery Charge (Note 6)	Q_{RR}			0		

All measurements were done with substrate connected to source.

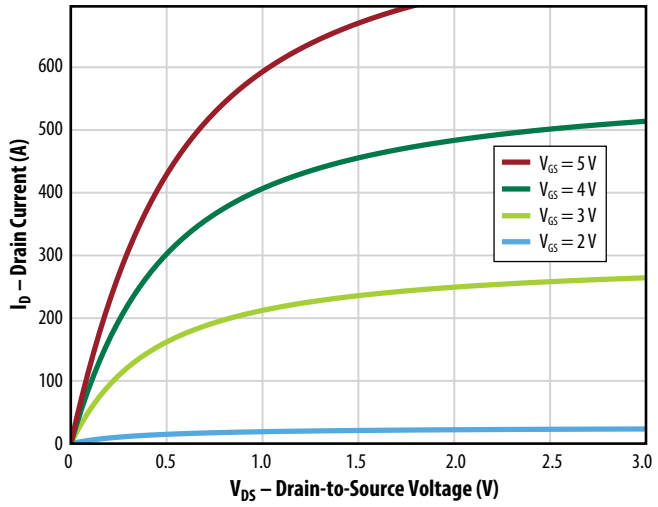


Figure 1: Typical Output Characteristics at 25°C

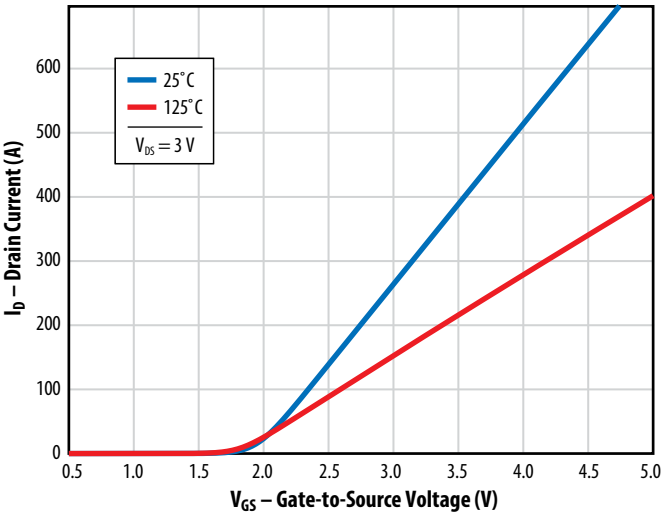


Figure 2: Typical Transfer Characteristics

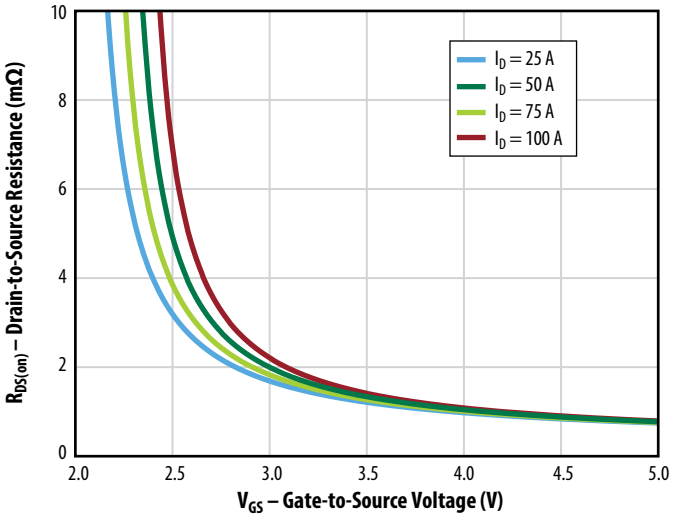


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

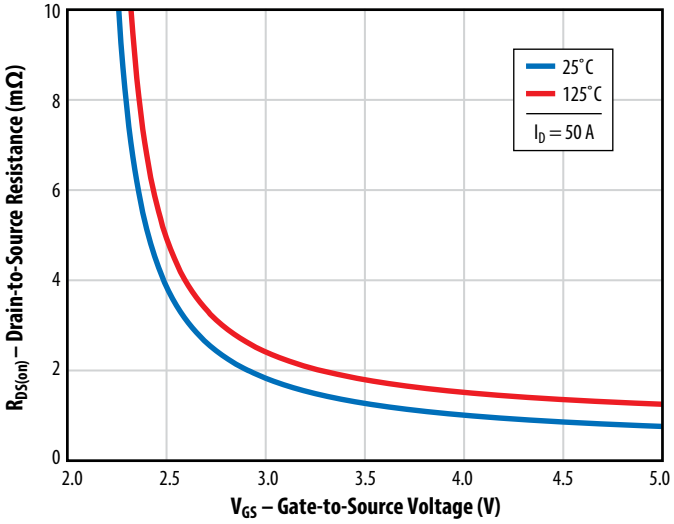


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

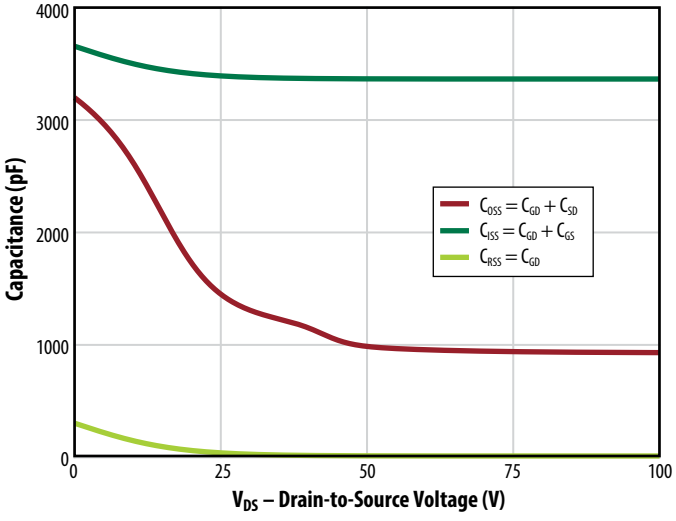


Figure 5a: Typical Capacitance (Linear Scale)

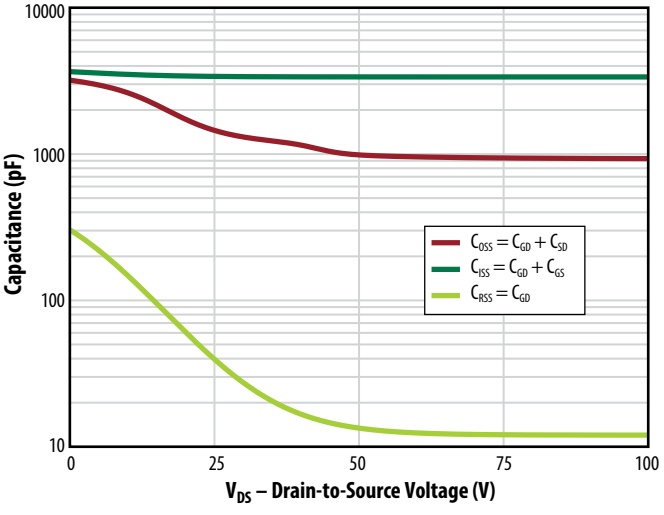


Figure 5b: Typical Capacitance (Log Scale)

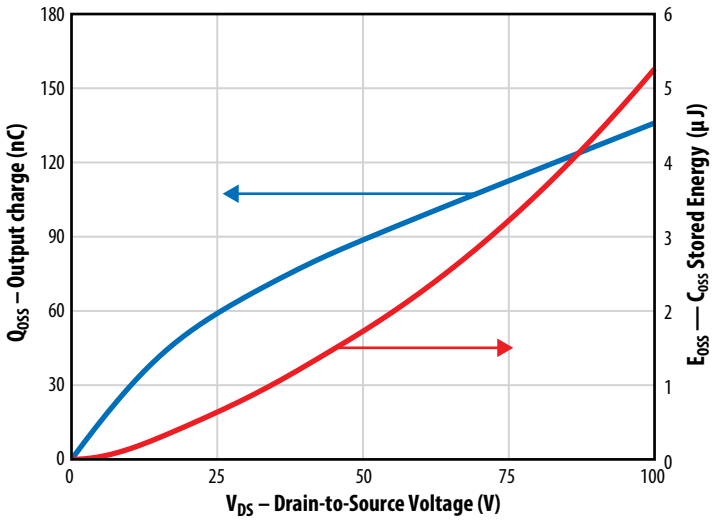


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

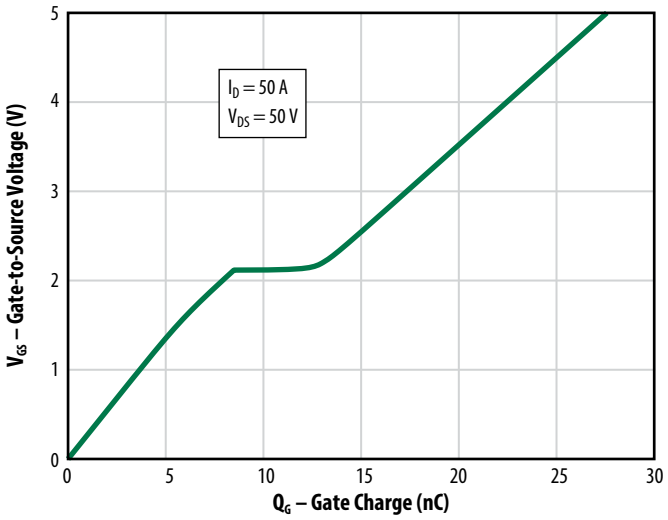


Figure 7: Typical Gate Charge

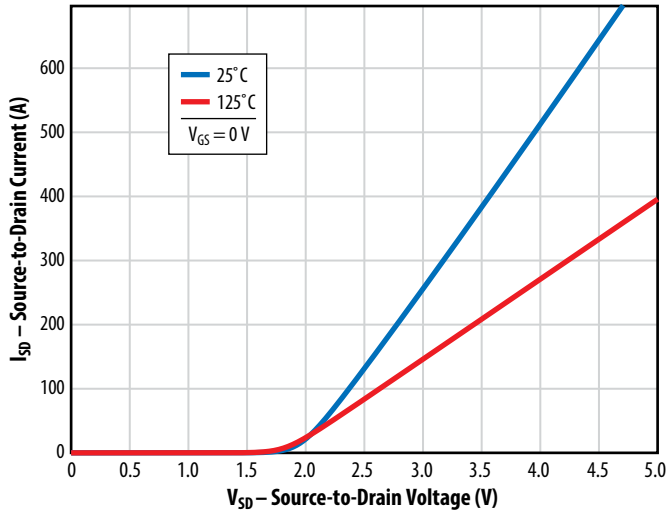


Figure 8: Typical Reverse Drain-Source Characteristics

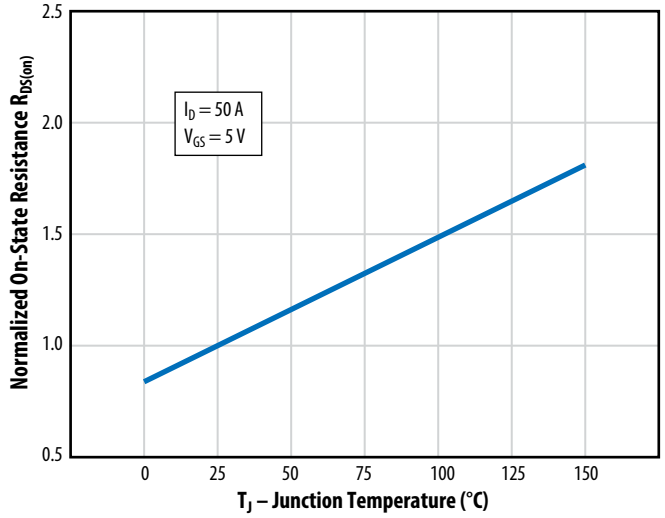


Figure 9: Typical Normalized On-State Resistance vs. Temperature

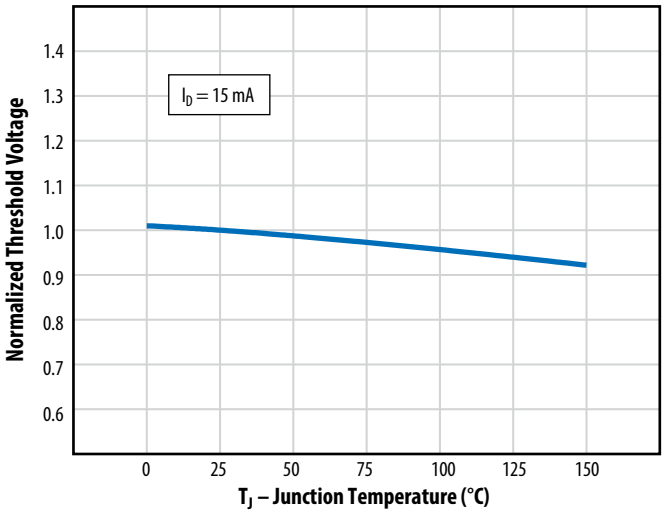


Figure 10: Typical Normalized Threshold Voltage vs. Temperature

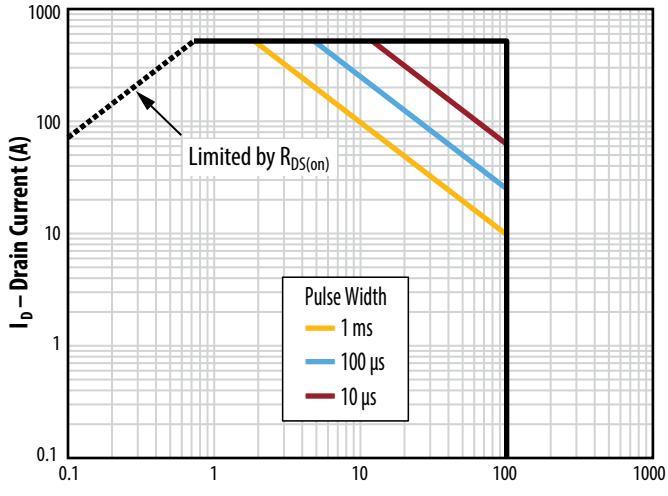


Figure 11: Safe Operating Area

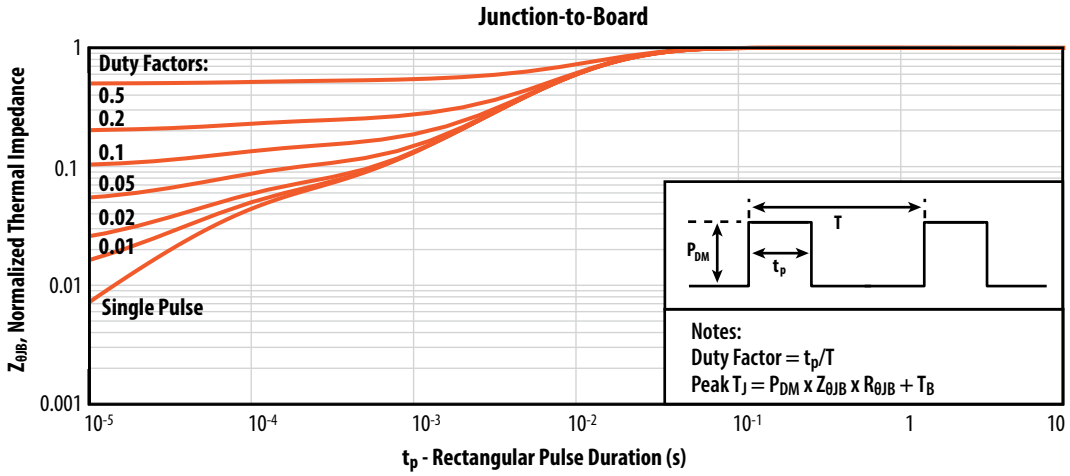


Figure 12: Typical Transient Thermal Response Curves

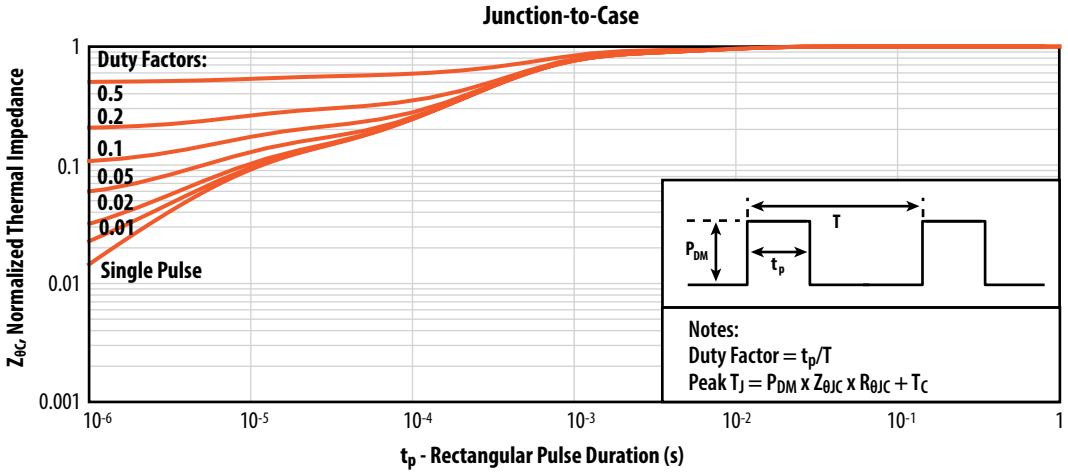
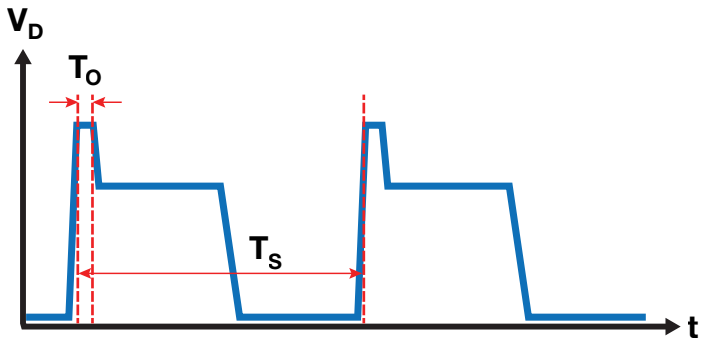


Figure 13: Typical Transient Thermal Response Curves



1% is the ratio between T_O (overvoltage duration) and T_S (one switching period).

Figure 14: Duty Cycle Factor (DC_{Factor}) Illustration for Repetitive Overvoltage Specification

Layout Characteristics

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

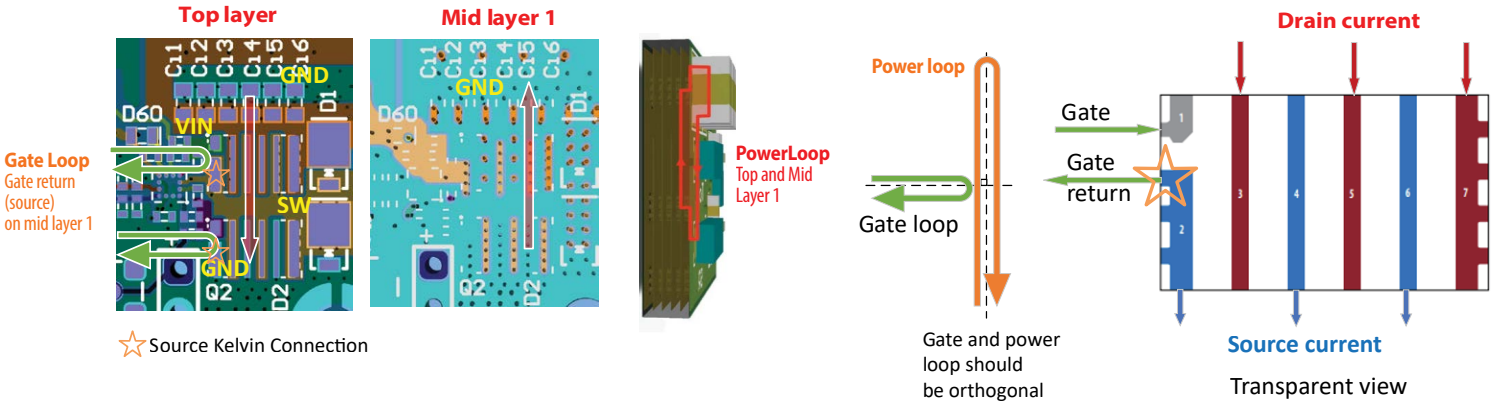


Figure 15: Inner Vertical Layout for Power and Gate Loops from EPC90156

Detailed recommendations on layout can be found on EPC's website: Optimizing PCB Layout with eGaN FETs.pdf

Typical Switching Behavior

The following typical switching waveforms are captured in these conditions:

- Gate driver: uP1966E with 0.4Ω/0.7Ω Pull-Down/Pull-Up Resistance
- External $R_G(ON)$ = 1 Ω, $R_{G(OFF)}$ = 0 Ω
- V_{IN} = 48 V, I_L = 30 A

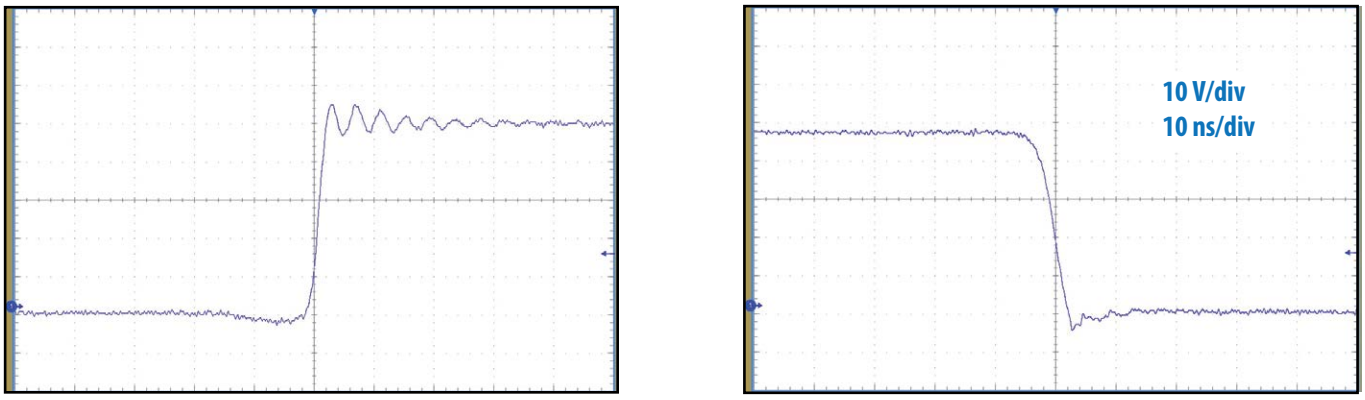


Figure 16: Typical half-bridge voltage switching waveforms

Typical Thermal Concept

The EPCS5007PAC can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

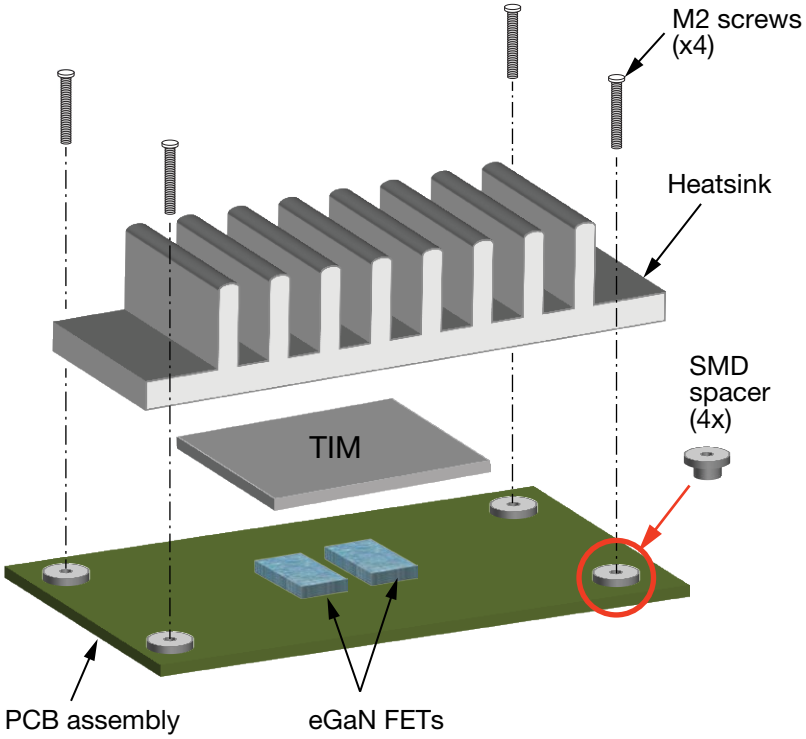


Figure 17: Exploded view of heatsink assembly using screws

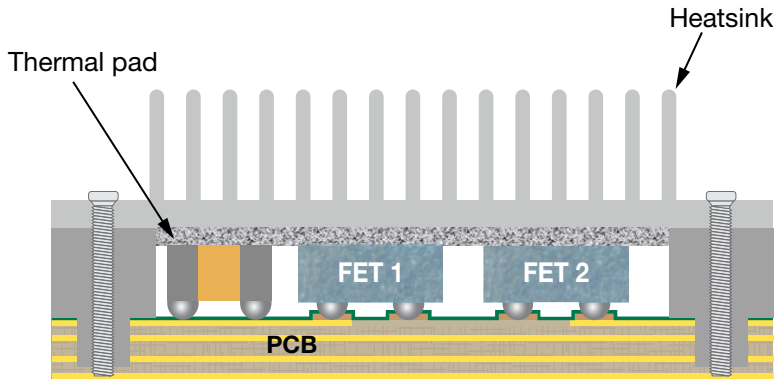


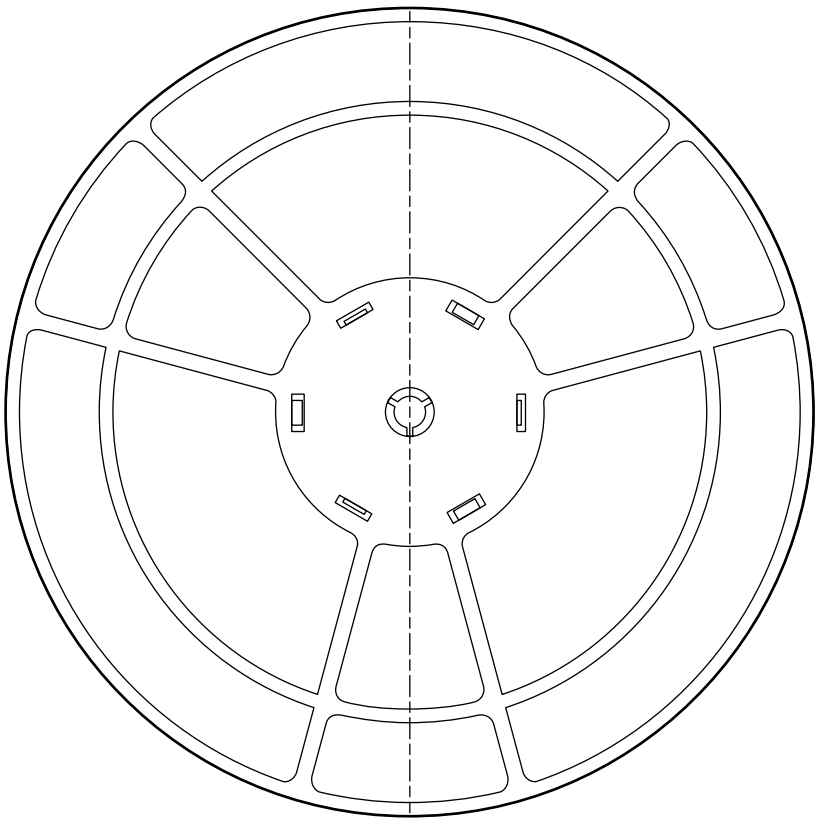
Figure 18: A cross-section image of dual sided thermal solution

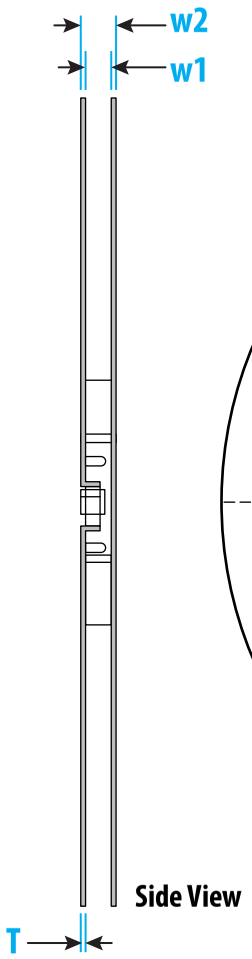
Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

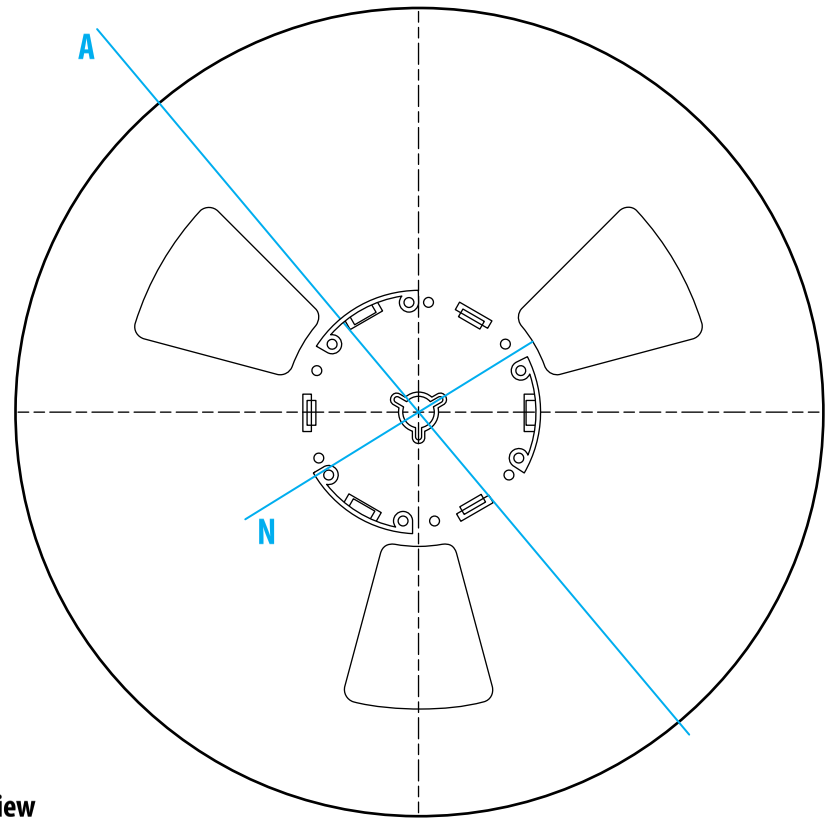
The thermal design can be optimized by using the **GaN FET Thermal Calculator** on EPC's website.

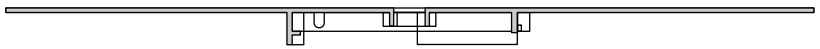
TAPE AND REEL

(units in mm)

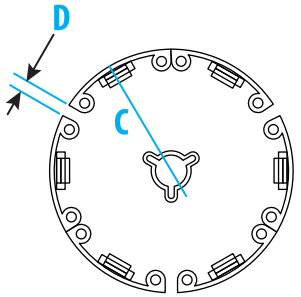




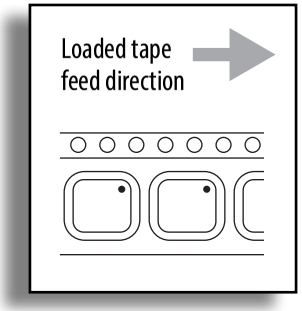




Top View Detail

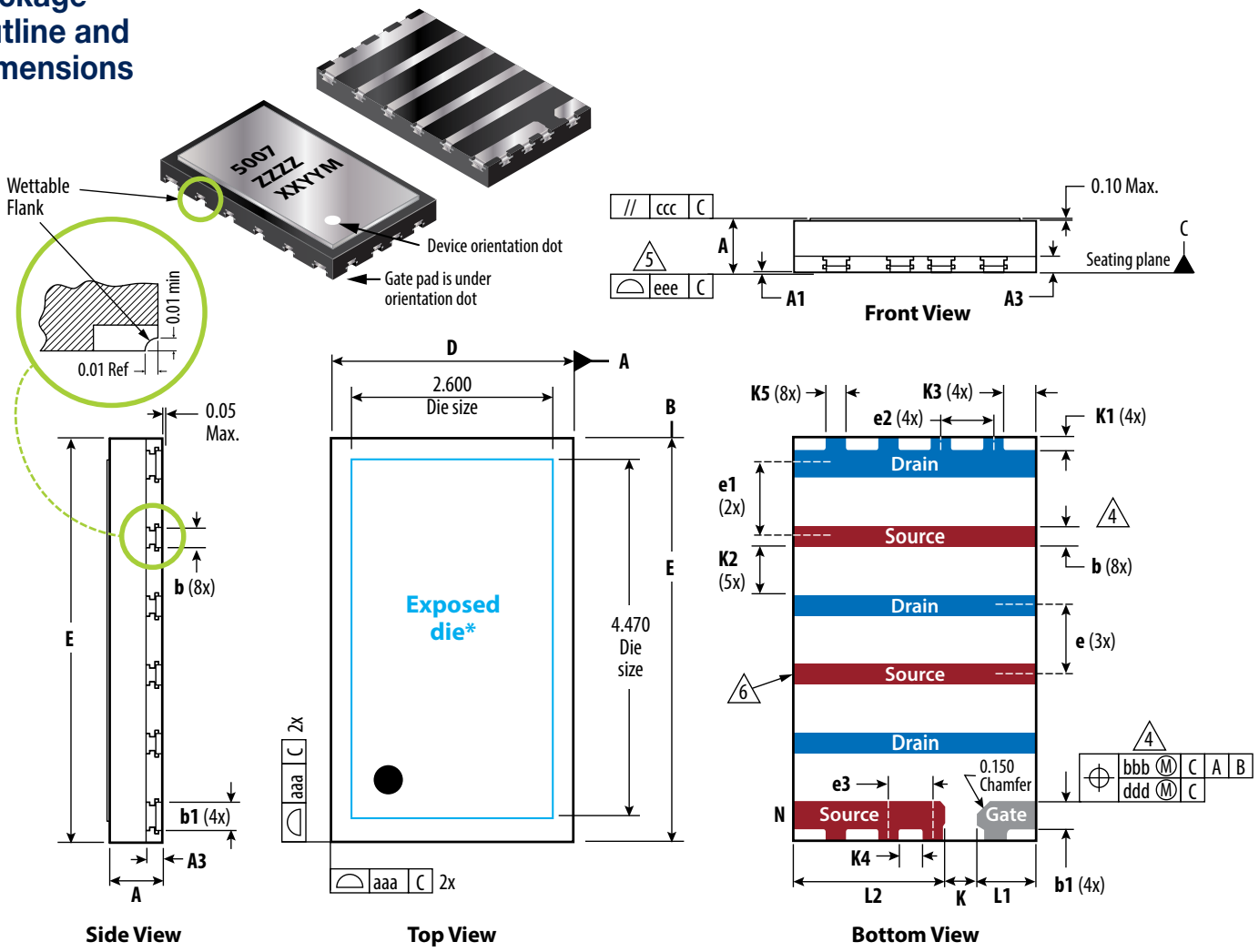


Bottom View Detail



Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5

Package Outline and Dimensions



*The exposed die is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

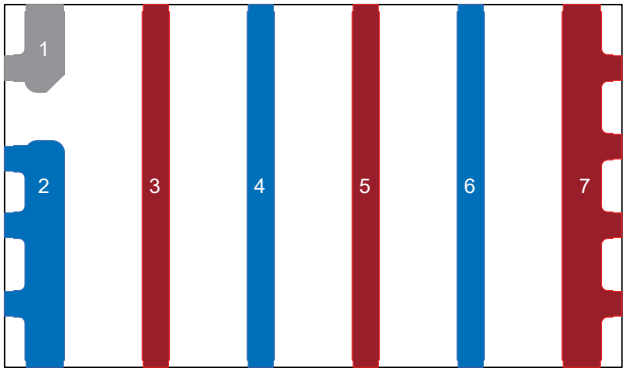
Symbol	Dimension (mm)			Note
	MIN	NOM	MAX	
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
D	2.90	3.00	3.10	
E	4.90	5.00	5.10	
e	0.85 BSC			
e1	0.90 BSC			
e2	0.65 BSC			
e3	0.55 BSC			
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

Symbol	Dimension (mm)			Note
	MIN	NOM	MAX	
K		0.40 Ref		
K1		0.15 Ref		
K2		0.60 Ref		
K3		0.40 Ref		
K4		0.30 Ref		
K5		0.25 Ref		
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		7		3

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metalized terminal and a radius on the other end of it, dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.
6. Lead plating is NiPdAu (1.5/0.01/0.005 µm min.) Au as the finish.

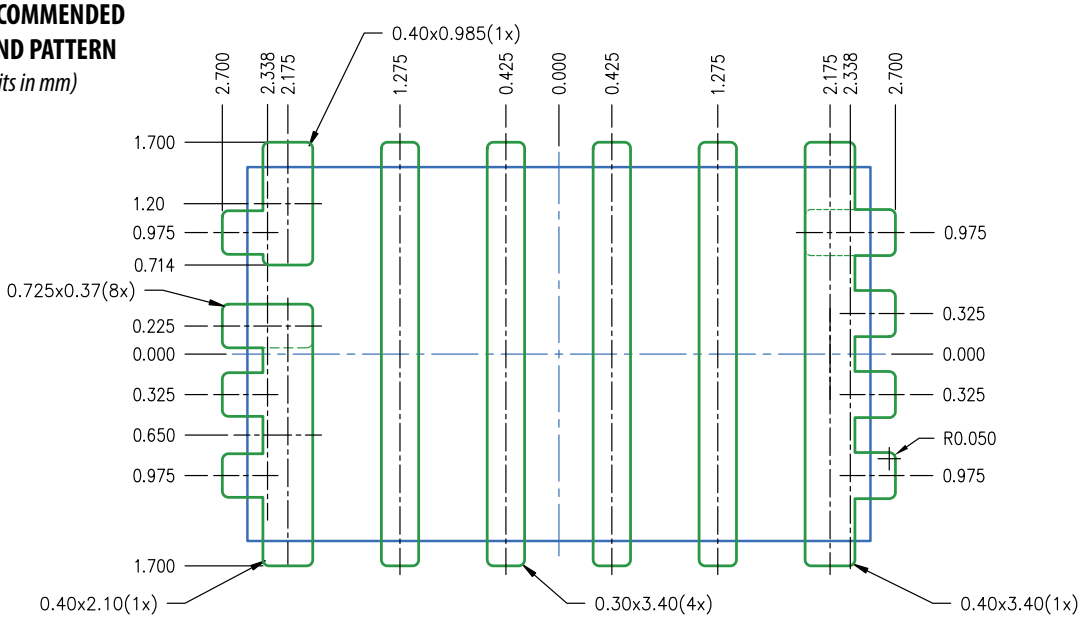
TRANSPARENT VIEW



PIN	Description
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Legend:

Part outline

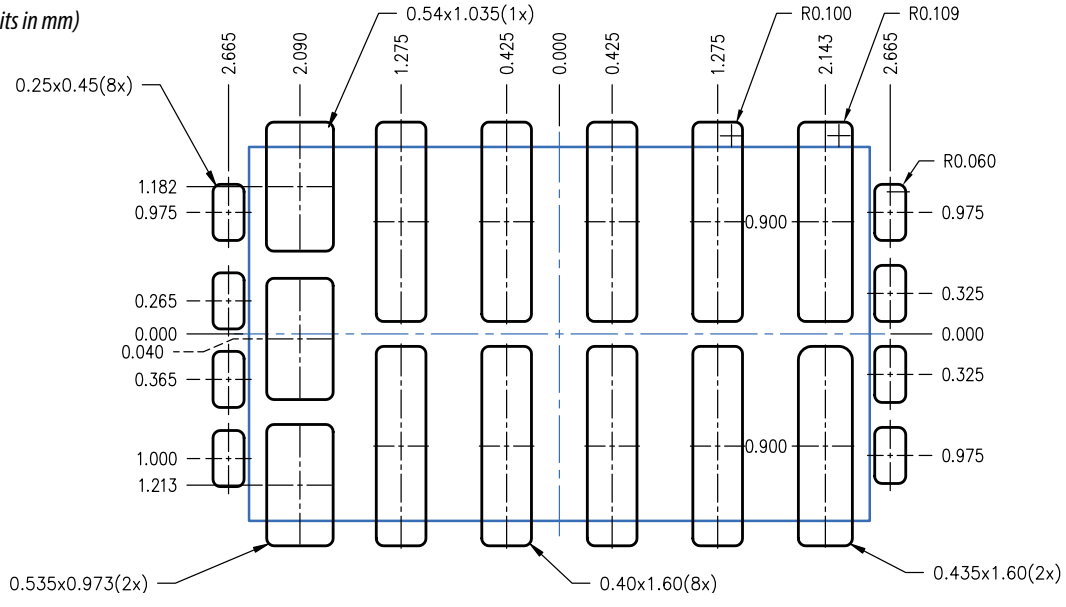
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



Legend:

Part outline

Stencil opening

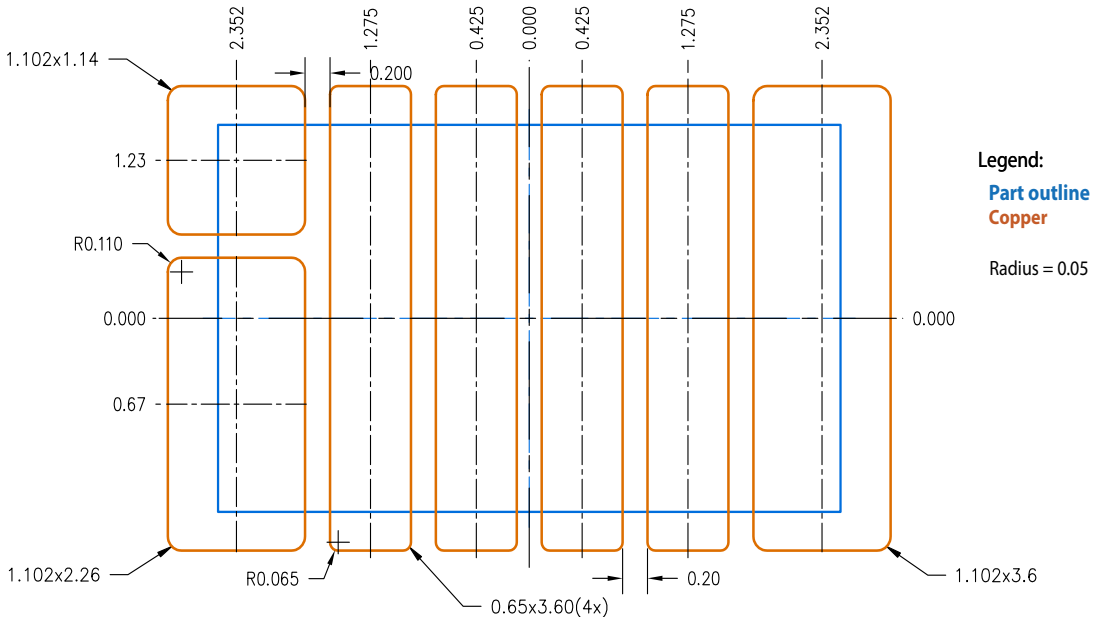
Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

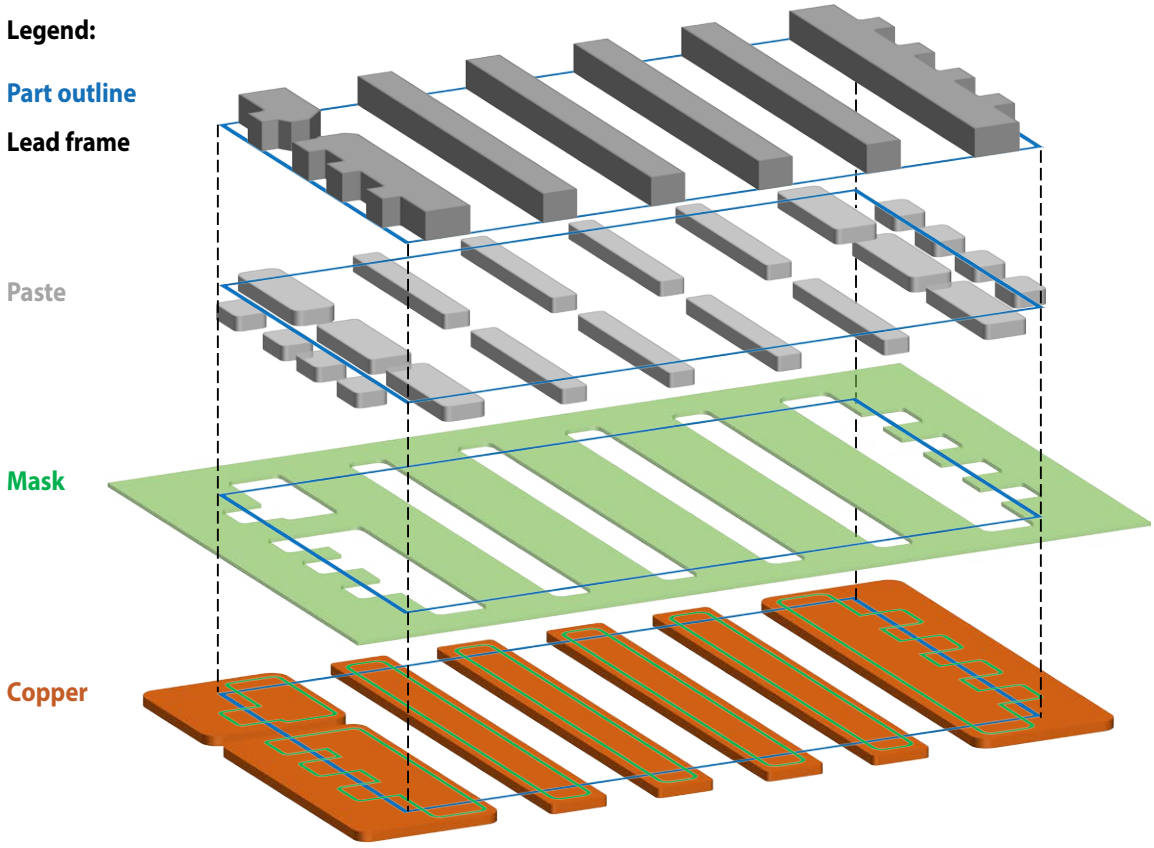
EPC has tested this stencil design and not found any scooping issues.

RECOMMENDED COPPER DRAWING

(units in mm)



3D COMPOSITE



ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

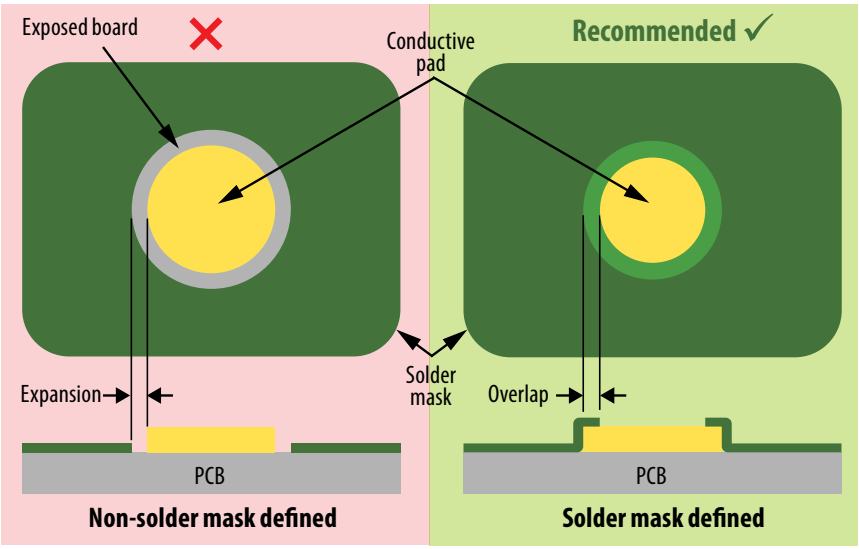


Figure 19: Solder mask defined versus non-solder mask defined pad

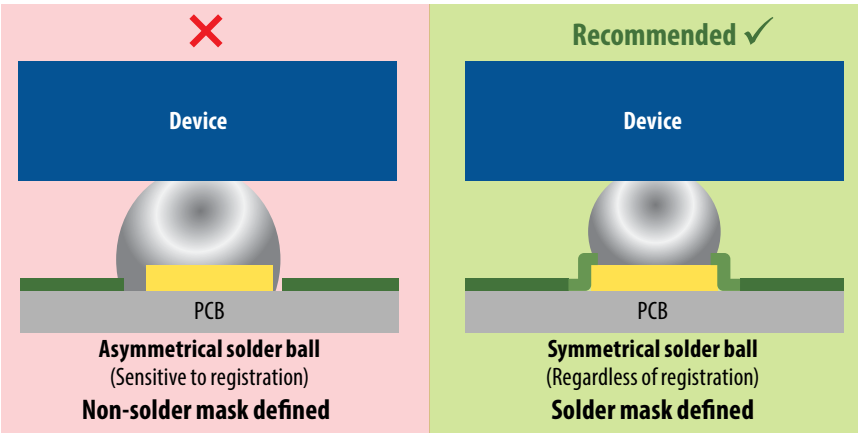


Figure 20: Effect of solder mask design on the solder ball symmetry

Additional Resources Available

- Assembly resources: https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs:
  https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip
  (for preliminary device Altium footprints, contact EPC Space)

Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.

Note 3. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 4. $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 5. $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 6. Guaranteed by design/device construction. Not Tested.

Note 7. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on})is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

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Change Log

Status	Version	Date	Remark
1.0	Preliminary	24 February 2026	Preliminary Release