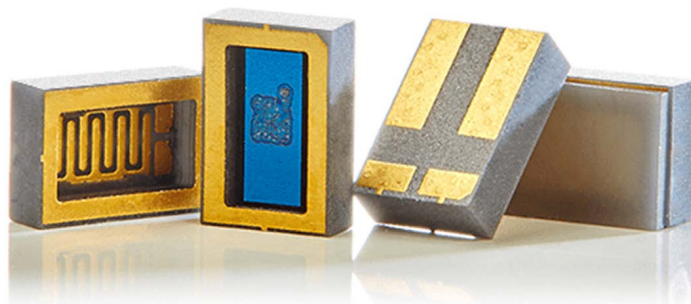


Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight – 0.160 grams
- Low $R_{DS(on)}$
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR and HDR Immune
- Single Event Effect (SEE) Hardened
 - SEE immunity up to LET of 37 MeV/(mg/cm²) in Si with V_{DS} up to 80% of rated Breakdown
- Neutron
 - Maintains Pre-Rad specification for up to 3×10^{15} Neutrons/cm²



EPCS9001DV

eGaN® FET in a Surface Mount (FSMD-D)
100 V, 90 A, 2.2 mΩ

Description

EPC Space FSMD-D series of eGaN® power switching HEMTs have been specifically designed for critical applications in the high reliability or commercial satellite space environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Applications

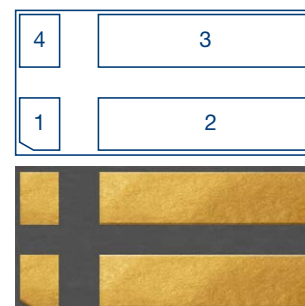
- High power density DC-DC converters
- Isolated power supplies
- Class-D amplifiers
- Low inductance motor drive

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 3)	48	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.05	

I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	SS	Source Sense



Absolute Maximum Rating ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain-to-Source Voltage (Note 1)	100	V
I_D	Continuous ($T_A = 25^\circ\text{C}$)	90	A
I_{DM}	Single-Pulse Drain Current $T_{pulse} \leq 80 \mu\text{s}$	390	
V_{GS}	Gate-to-Source Voltage (Note 2)	6 / -4	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_{sol}	Package Mounting Surface Temperature	260	

Static Characteristics (*Typical (TYP) values are for reference only.*)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
B_{VDSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$		20	200	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 6\text{ V}, T_J = 25^\circ\text{C}$		0.02	4	mA
	Gate-to-Source Forward Leakage	$V_{GS} = 6\text{ V}, T_J = 125^\circ\text{C}$		0.1	9	mA
I_{GSSR}	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		20	200	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 14\text{ mA}$	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance (Note 4)	$V_{GS} = 5\text{ V}, I_D = 90\text{ A}$		1.8	2.2	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.5		V

Dynamic Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. *Typical (TYP) values are for reference only.*)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Units
C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1610	1940	pF
C_{RSS}	Reverse transfer Capacitance			15		
C_{OSS}	Output Capacitance			1100	1650	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 5)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		1450		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 6)			1790		
R_G	Gate Resistance (Note 7)			0.3		Ω
Q_G	Total Gate Charge (Note 8)	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 50\text{ A}$		15	19	nC
Q_{GS}	Gate to Source Charge (Note 8)	$V_{DS} = 50\text{ V}, I_D = 50\text{ A}$		4.1		
Q_{GD}	Gate to Drain Charge (Note 8)			3		
$Q_{G(TH)}$	Gate Charge at Threshold (Note 7)			2.7		
Q_{OSS}	Output Charge (Note 7)	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		72	108	
Q_{RR}	Source to Drain Recovery Charge (Note 7)			0		

All measurements were done with substrate connected to source.

Figure 1: Typical Output Characteristics at 25°C

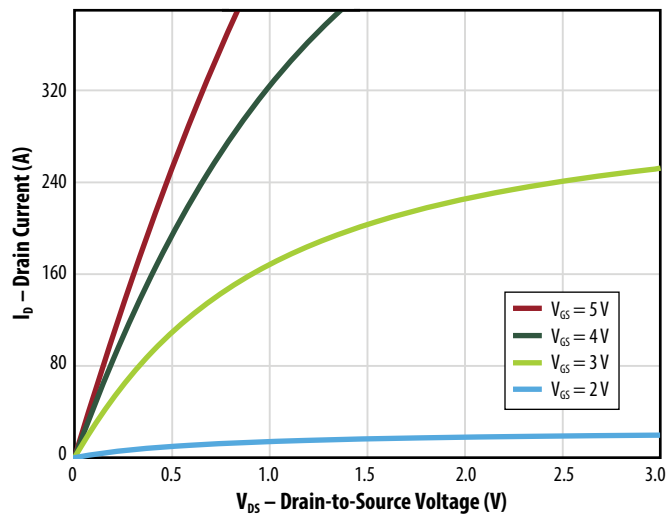


Figure 2: Typical Transfer Characteristics

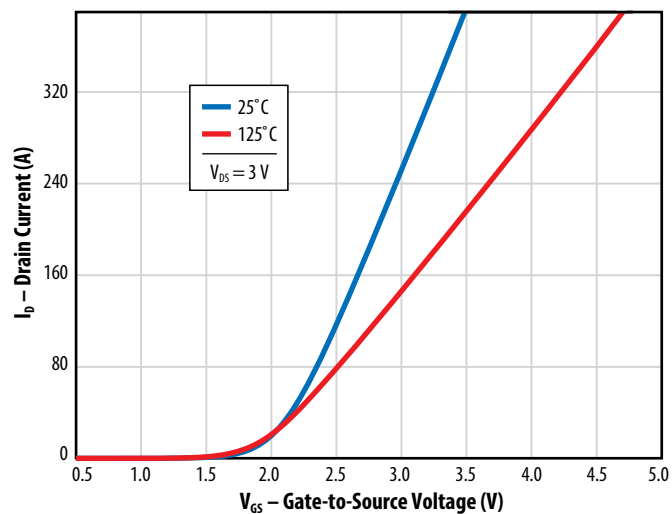
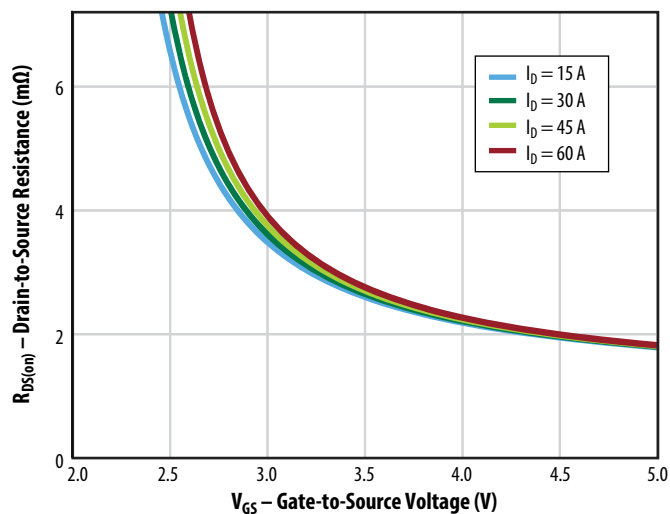
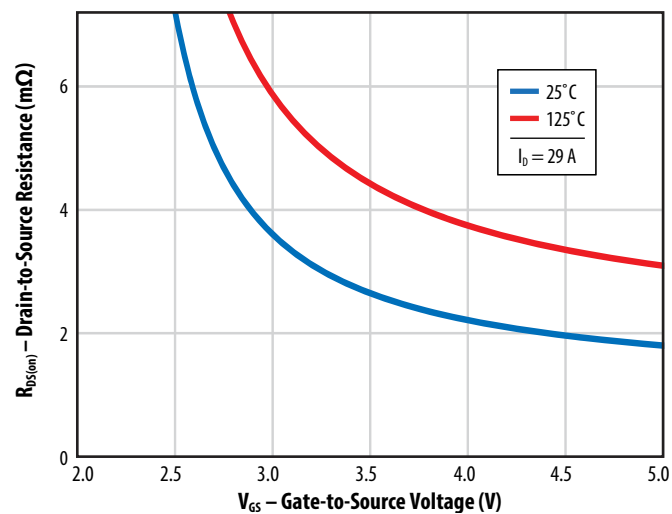
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

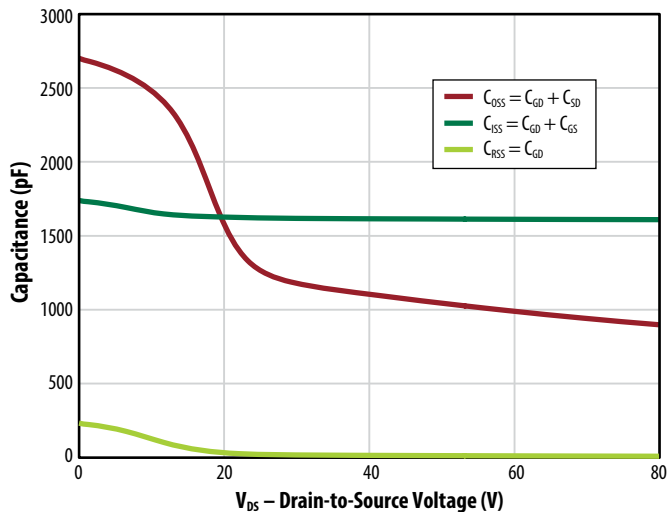


Figure 5b: Typical Capacitance (Log Scale)

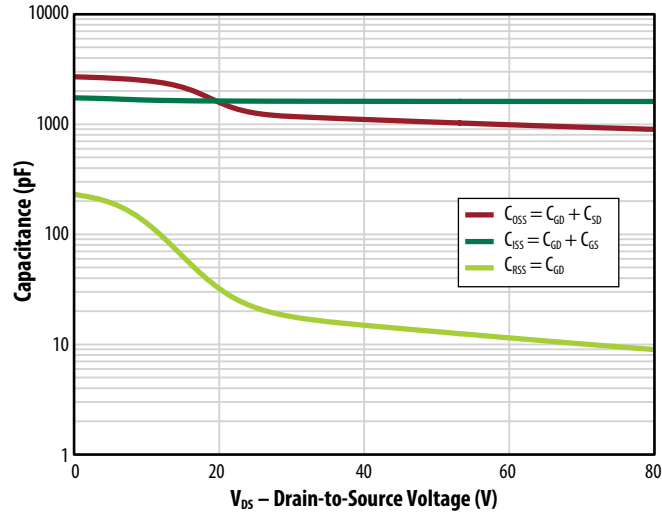


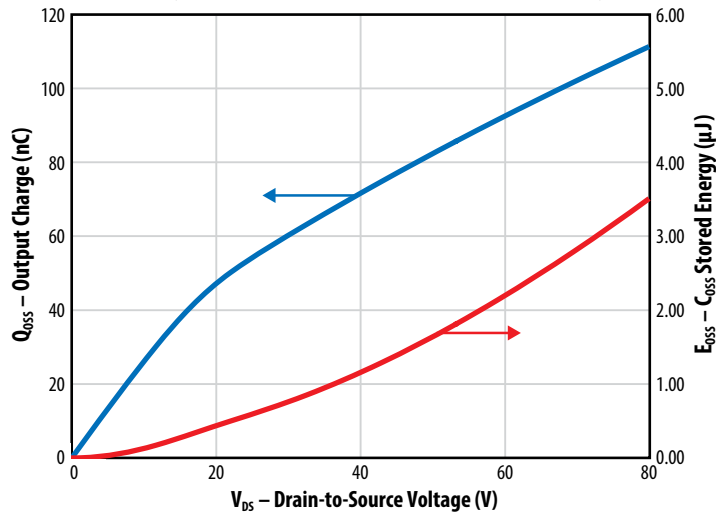
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

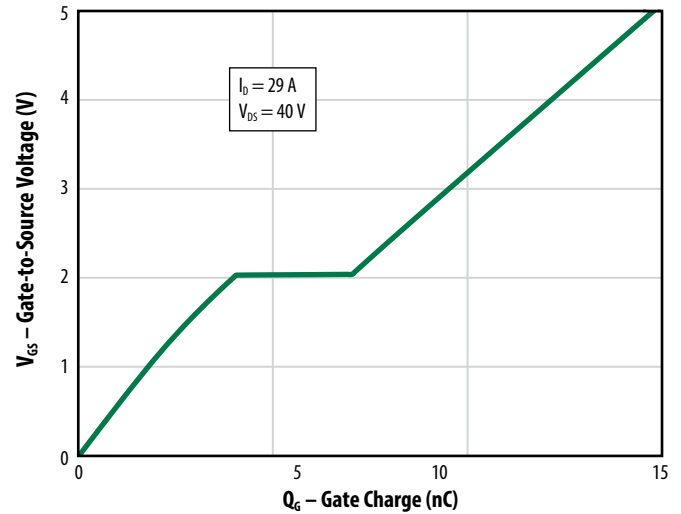


Figure 8: Typical Reverse Drain-Source Characteristics

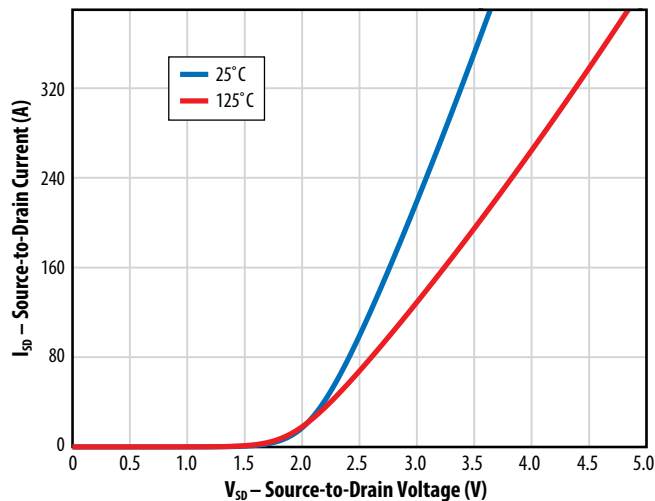


Figure 9: Typical Normalized On-State Resistance vs. Temp.

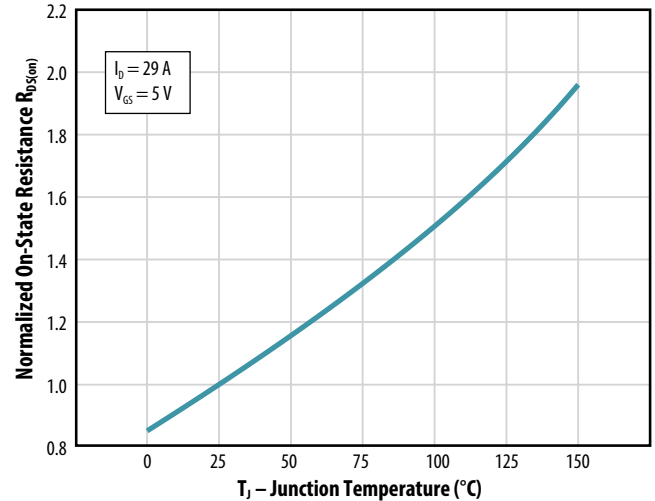


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

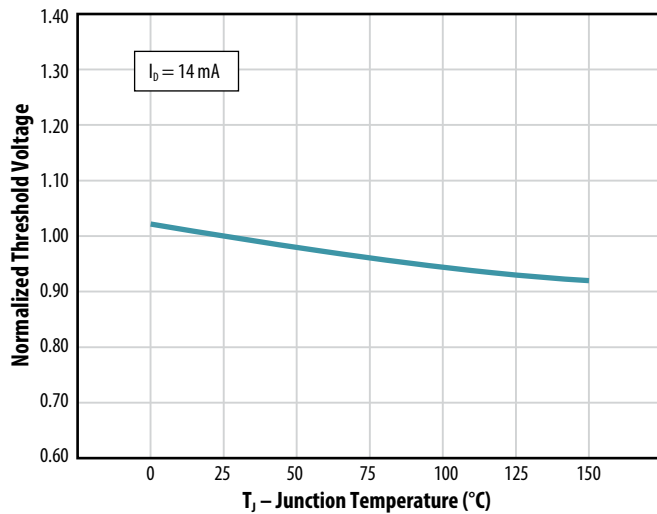
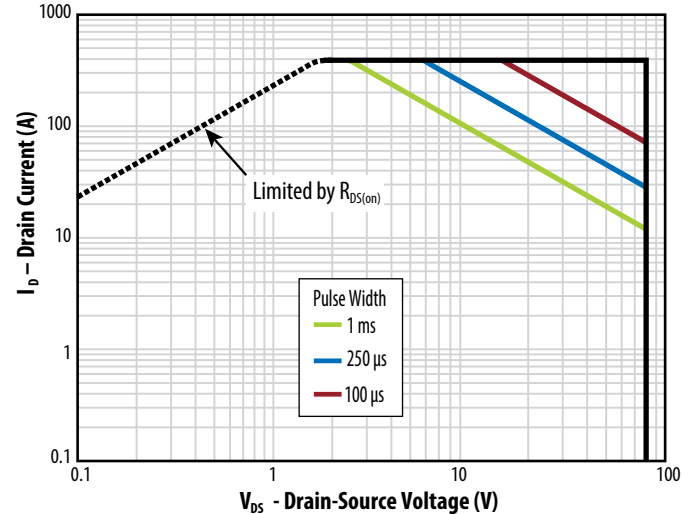


Figure 11: Safe Operating Area



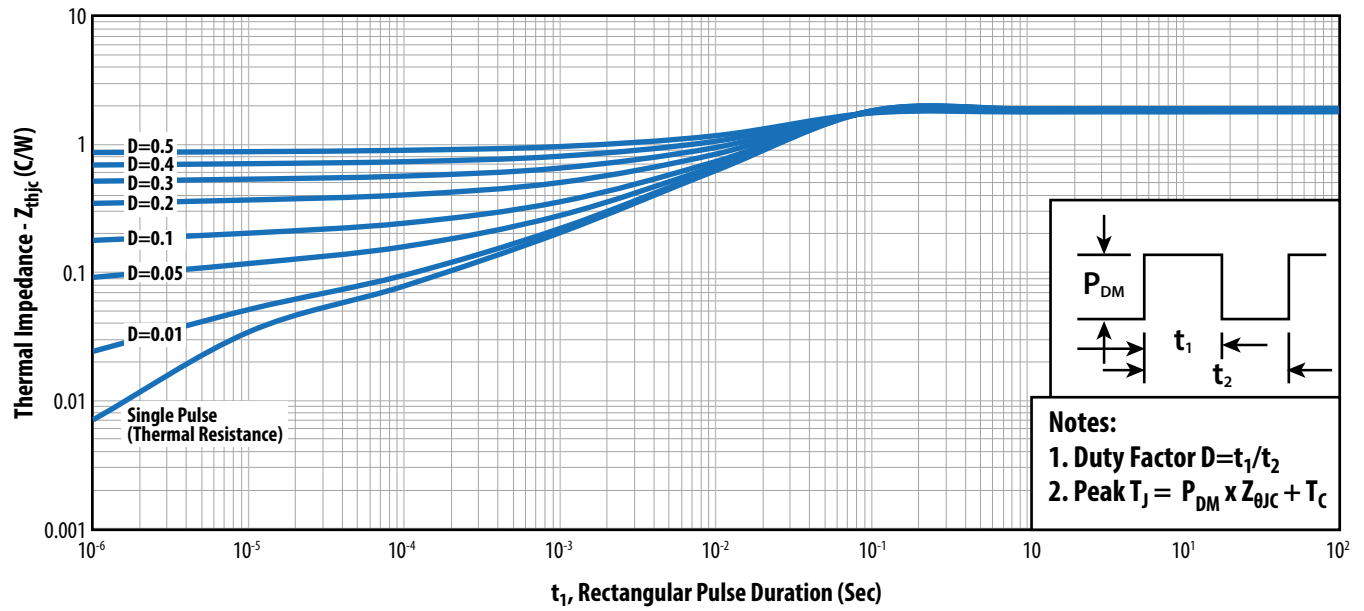
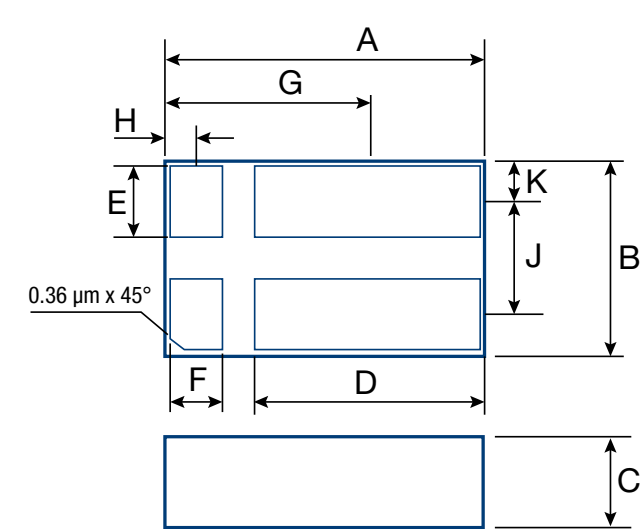


Figure 12: Thermal Impedance diagram

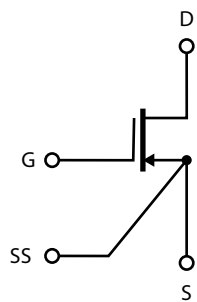
Package Outline and Dimensions



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
A	0.311	0.321	7.90	8.15	
B	0.177	0.187	4.50	4.75	
C	0.078	0.088	1.98	2.24	
D	0.222	0.232	5.64	5.89	
E	0.065	0.075	1.65	1.91	
F	0.045	0.055	1.14	1.40	
G	0.195	0.205	4.95	5.21	
H	0.025	0.035	0.64	0.89	
K	0.035	0.045	0.89	1.14	
J	0.095	0.105	2.41	2.67	

Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb.

Package Connections



NOTE: SS pin is connected directly to source of internal die.

Notes

- Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.
- Note 3: $R_{\theta JA}$ measured with FSMD-D package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 μ s and duty cycle is 1%, maximum..
- Note 5. $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .
- Note 6. $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .
- Note 7. Guaranteed by design/device construction. Not tested.
- Note 8. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S . The gate current is adjusted to yield the desired charge per unit time ($I_{const} \cdot \text{time per division}$) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off}/t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC} .

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