## Features

- Low $R_{DS(on)}$
- Ultra-low $Q_G$ For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 83.2 MeV/(mg/cm$^2$) in Si with $V_{DS}$ up to 100% of rated Breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 4 x $10^{15}$ Neutrons/cm$^2$

## Applications

- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers

## FBG04N30BSH

**Rad-Hard eGaN® 40 V, 30 A,**
**11 mΩ Surface Mount (FSMD-B)**

## Description

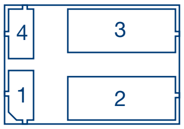
EPC Space FSMD-B series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge ($Q_G$) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

### Thermal Characteristics

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient (Note 3) | 48 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance Junction to Case | 2.7 | |

### I/O Pin Assignment *(Bottom View)*

| Pin | Symbol | Description |
|---|---|---|
| 1 | G | Gate |
| 2 | D | Drain |
| 3 | S | Source |
| 4 | SS | Source Sense |




### Absolute Maximum Rating *($T_C$ = 25°C unless otherwise noted)*

| Symbol | Parameter-Conditions | Value | Units |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage (Note 1) | 48 | V |
| $I_D$ | Continuous Drain Current ID @ $V_{GS}$ = 4.5 V, $T_C$ = 25°C | 30 | A |
| $I_{DM}$ | Single-Pulse Drain Current $t_{pulse} \leq 80$ µs | 120 | |
| $V_{GS}$ | Gate to Source Voltage (Note 2) | +6 / -4 | V |
| $T_J$ , $T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150 | °C |
| $T_{sol}$ | Package Mounting Surface Temperature | 260 | |
| ESD | ESD Class | 1A (ΔA) | |
| Weight | Device Weight | 0.135 | g |

### Electrical Characteristics *($T_C$ = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

| Parameter | Symbol | Test Conditions | | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|---|
| Maximum Drain to Source Voltage | $V_{DSMAX}$ | $V_G$ = 0 V | | 40 | | | V |
| Drain to Source Leakage | $I_{DSS}$ | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | $T_C$ = 25°C | | 26 | 400 | μA |
| | | | $T_C$ = 125°C | | 300 | 1000 | μA |
| Gate to Source Forward Leakage | $I_{GSSF}$ | $V_{GS}$ = 6 V | $T_C$ = 25°C | | 100 | 500 | μA |
| Gate to Source Reverse Leakage | $I_{GSSR}$ | $V_{GS}$ = -4 V | $T_C$ = 25°C | | 50 | 400 | μA |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 5 mA | $T_C$ = 25°C | 0.8 | 1 | 2.5 | V |
| Gate to Source Threshold Voltage Temperature Coefficient | $\Delta V_{GS(th)}/\Delta T$ | $V_{DS} = V_{GS}$, $I_D$ = 5 mA | -55°C < $T_A$ < 150°C | | \|1.5\| | | mV/°C |
| Drain to Source Resistance (Note 4) | $R_{DS(on)}$ | $I_D$ = 30 A, $V_{GS}$ = 5 V | $T_C$ = 25°C | | 9 | 11 | mΩ |
| Source to Drain Forward Voltage | $V_{SD}$ | $I_S$ = 0.5 A, $V_G$ = 0 V | $T_C$ = 25°C | | 2.5 | 3 | V |

### Dynamic Characteristics *($T_C$ = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{ISS}$ | f = 1 MHz, $V_{DS}$ = 20 V, $V_{GS}$ =0 V | | 1100 | 1300 | pF |
| Output Capacitance | $C_{OSS}$ | f = 1 MHz, $V_{DS}$ = 20 V, $V_{GS}$ =0 V | | 650 | 900 | pF |
| Reverse transfer Capacitance | $C_{RSS}$ | f = 1 MHz, $V_{DS}$ = 20 V, $V_{GS}$ =0 V | | 30 | 60 | pF |
| Gate Resistance (Note 5) | $R_G$ | f = 1 MHz, $V_{DS} = V_{GS}$ = 0 V | | 1.1 | | Ω |
| Total Gate Charge (Note 6) | $Q_G$ | $I_D$ = 30 A, $V_{GS}$ = 5 V, $V_{DS}$ = 20 V | | 8.9 | 11.4 | nC |
| Gate to Drain Charge (Note 6) | $Q_{GD}$ | $I_D$ = 30 A, $V_{GS}$ = 5 V, $V_{DS}$ = 20 V | | 2.1 | 3.0 | nC |
| Gate to Source Charge (Note 6) | $Q_{GS}$ | $I_D$ = 30 A, $V_{GS}$ = 5 V, $V_{DS}$ = 20 V | | 2.3 | 5.5 | nC |
| Output Charge (Note 5) | $Q_{OSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | | 22 | 26 | nC |
| Source to Drain Recovery Charge | $Q_{RR}$ | $I_D$ = 30 A, $V_{DS}$ = 20 V | | <1 | | nC |

## Radiation Characteristics

EPC Space eGaN® HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON | $V_{GS}$ = 5 V
NO BIAS | $V_{DS}$ = $V_{GS}$ = 0 V
OFF | $V_{DS}$ = 80% $B_{VDSS}$

### Electrical Characteristics up to 1000 krads *($T_C$ = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

| Parameter | Symbol | Test Conditions | MIN | TYP | MAX | Units |
|---|---|---|---|---|---|---|
| Maximum Drain to Source Voltage | $V_{DSMAX}$ | $V_{GS}$ = 0 V | 40 | | | V |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$ , $I_D$ = 5 mA | 0.8 | 1 | 2.5 | |
| Drain to Source Leakage | $I_{DSS}$ | $V_{DS}$ = 40 V, $V_{GS}$ = 0 V | | 26 | 400 | µA |
| Gate to Source Forward Leakage | $I_{GSSF}$ | $V_{GS}$ = 6 V | | 100 | 600 | |
| Gate to Source Reverse Leakage | $I_{GSSR}$ | $V_{GS}$ = -4 V | | 50 | 400 | |
| Drain to Source Resistance (Note 4) | $R_{DS(on)}$ | $I_D$ = 30 A, $V_{GS}$ = 5 V | | 9 | 11 | mΩ |

## Typical Single Event Effect Safe Operating Area

*Note: All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.*

| Test | Environment | | | | $V_{DS}$ Voltage ( V) | |
|---|---|---|---|---|---|---|
| See SOA | Ion | LET MeV(mg/cm²) in Si (+/-5%) | Range µm (+/- 7.5%) | Energy MeV (+/-10%) | $V_{GS}$ = 0 V | $V_{GS}$ = -4V |
| | Xe | 63.6 | 71.3 | 963 | 40 | 40 |
| | Au | 83.2 | 121.4 | 2256 | 40 | 40 |

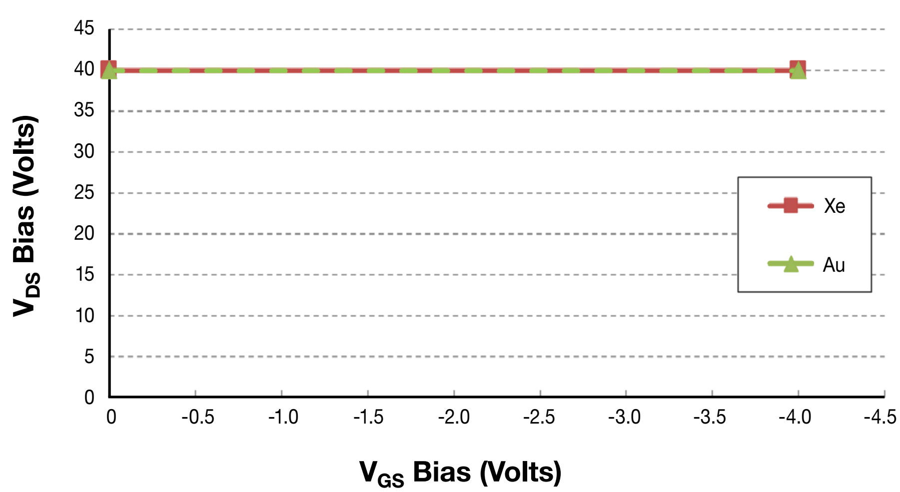



*Figure 1. Typical Single Event Effect Safe Operating Area*

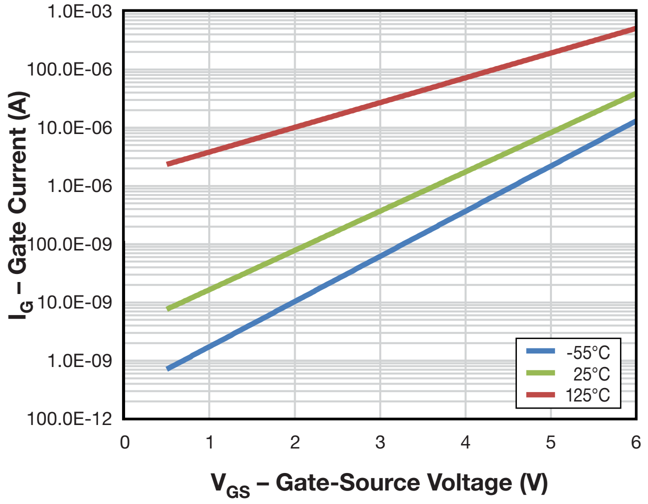



*Figure 2. Typical Gate-Source Leakage Current vs. Ambient Temperature*

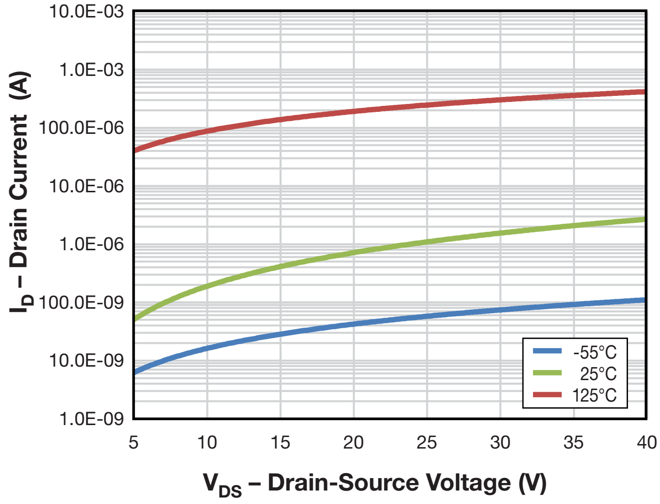



*Figure 3. Typical Drain-Source Leakage Current vs. Ambient Temperature*

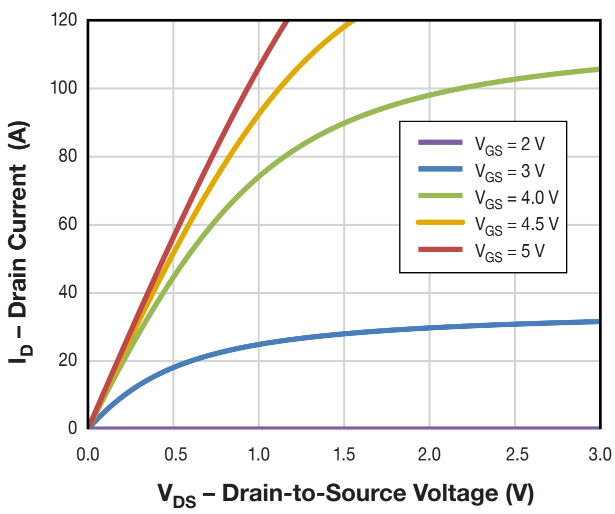



*Figure 4. Typical Output Characteristics at 25 °C*

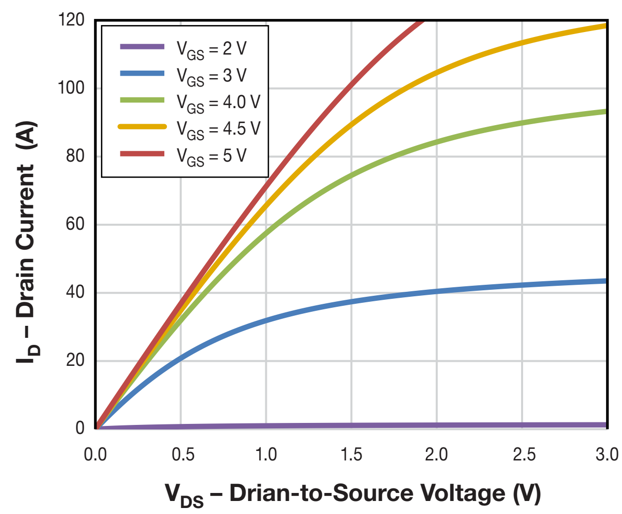



*Figure 5. Typical Output Characteristics at 125 °C*

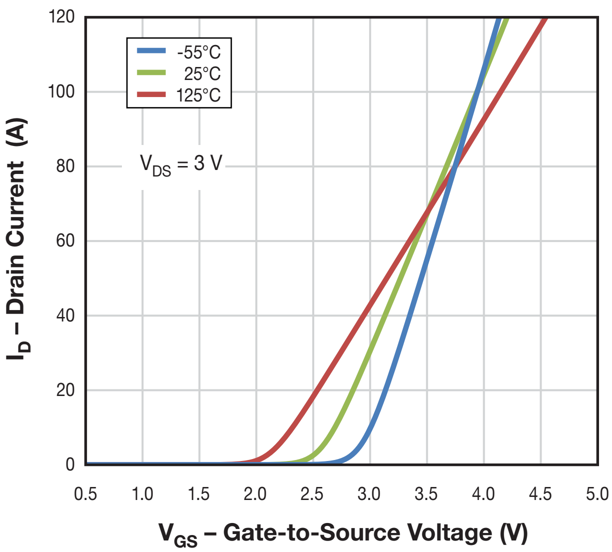



*Figure 6. Typical Transfer Characteristics*

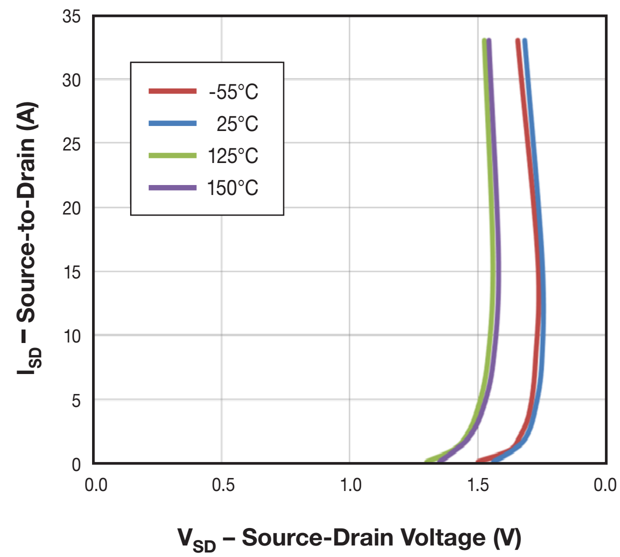



*Figure 7. Reverse Drain-Source Characteristics*

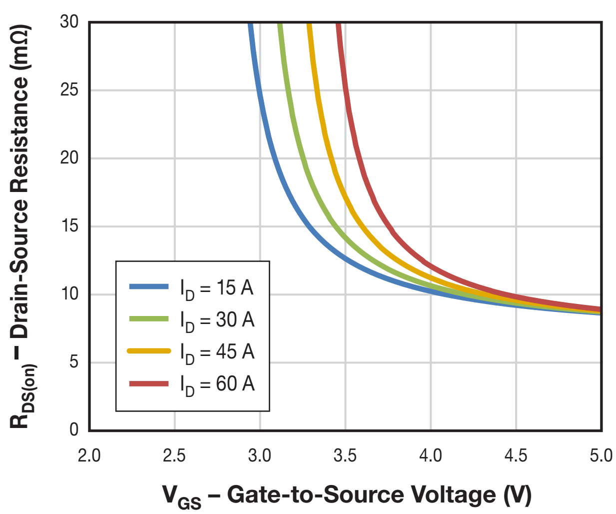



*Figure 8. $R_{DS(on)}$ vs $V_{GS}$ for Various Drain Currents*

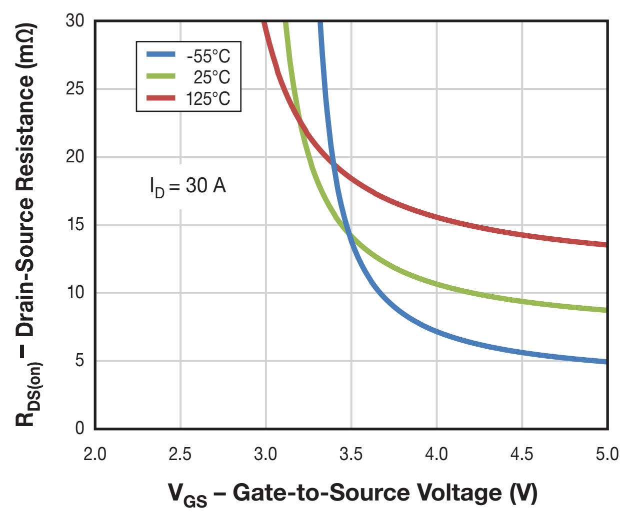



*Figure 9. $R_{DS(on)}$ vs $V_{GS}$ for Various Temperatures*

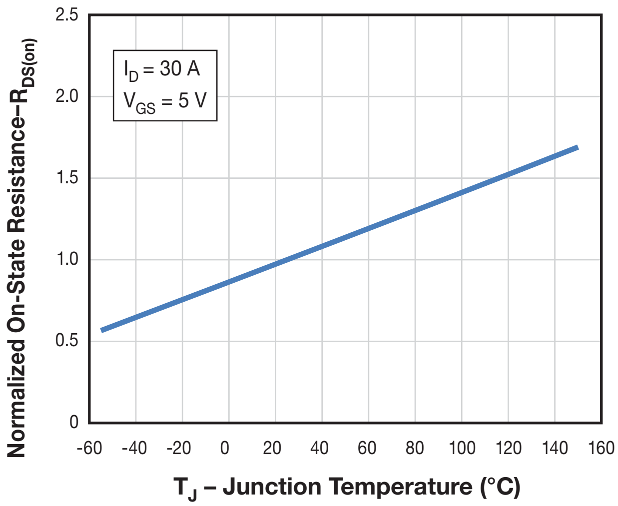



*Figure 10. Normalized On-State Resistance vs. Temperature*

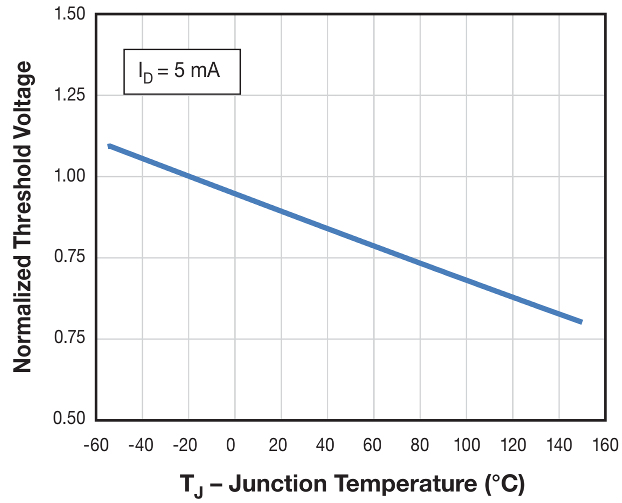



*Figure 11. Normalized Threshold Voltage vs. Temperature*

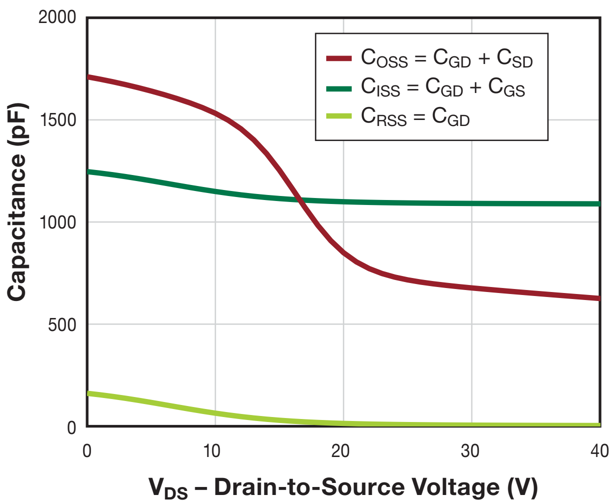



*Figure 12. Typical Capacitance*

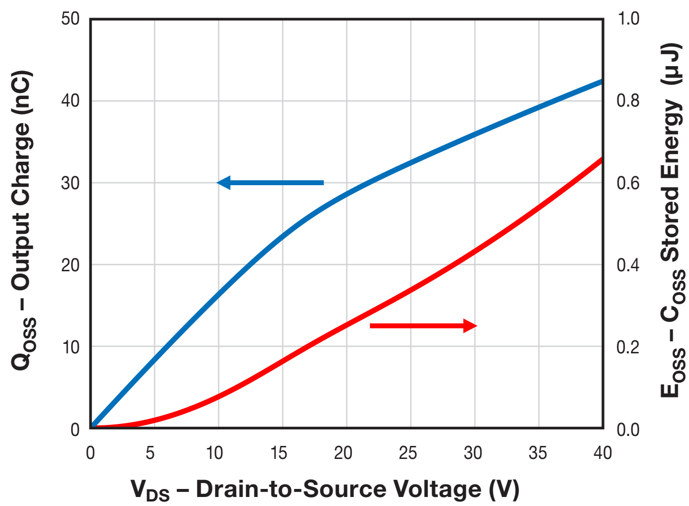



*Figure 13. Typical Output Charge and $C_{OSS}$ Stored Energy*

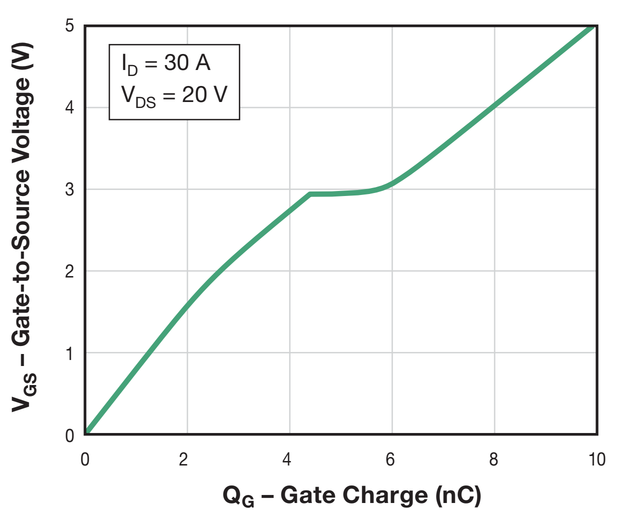



*Figure 14. Typical Gate Charge*

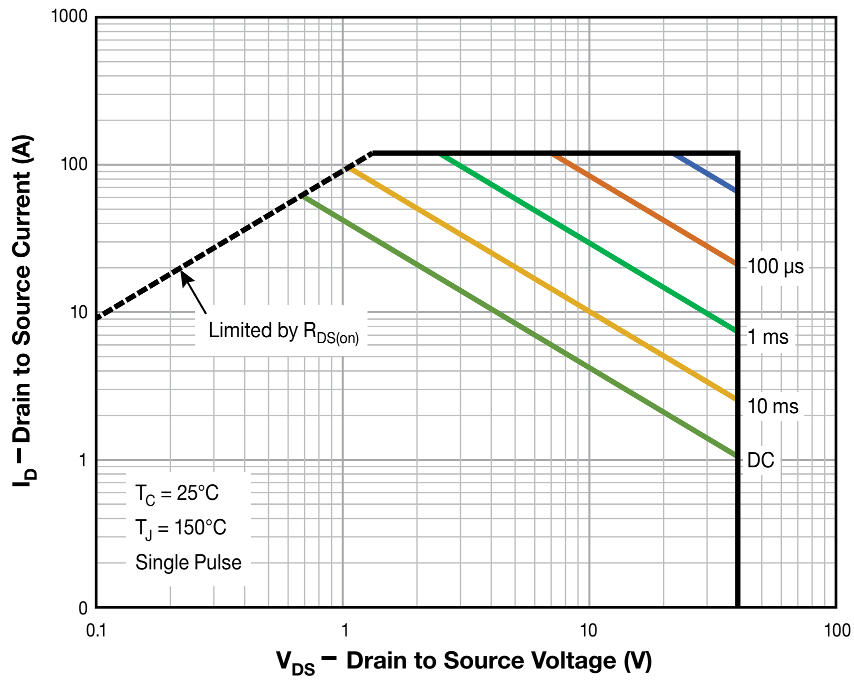



*Figure 15. Safe Operating Area*

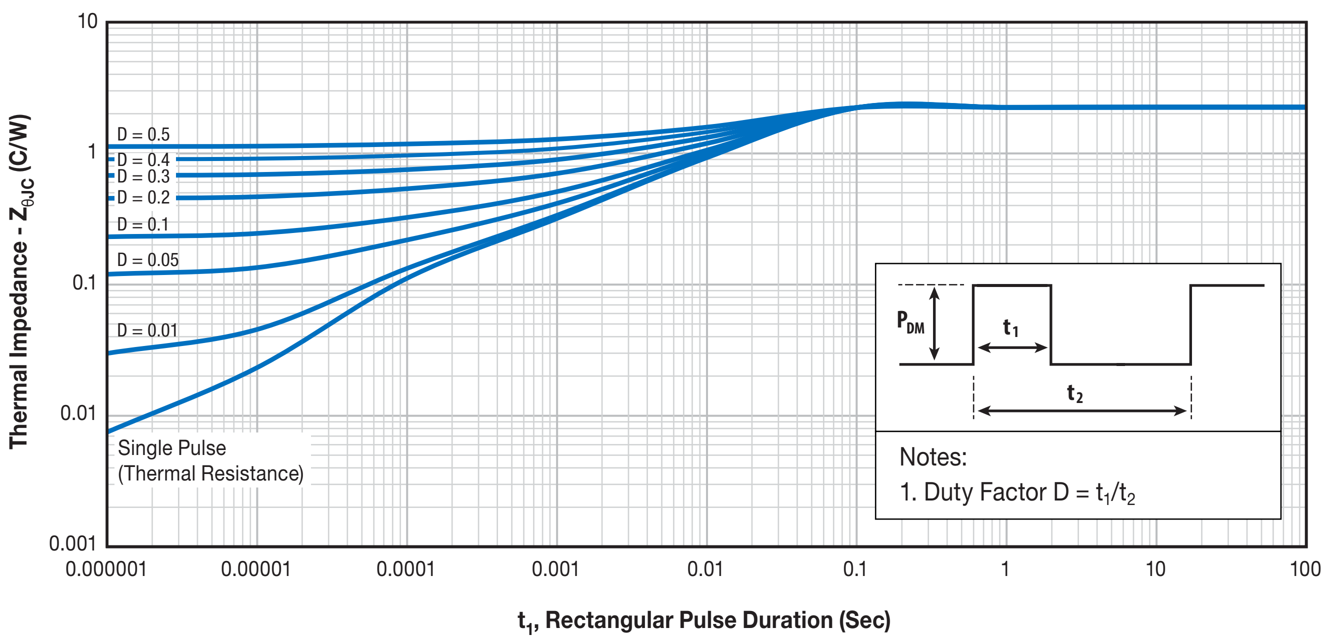
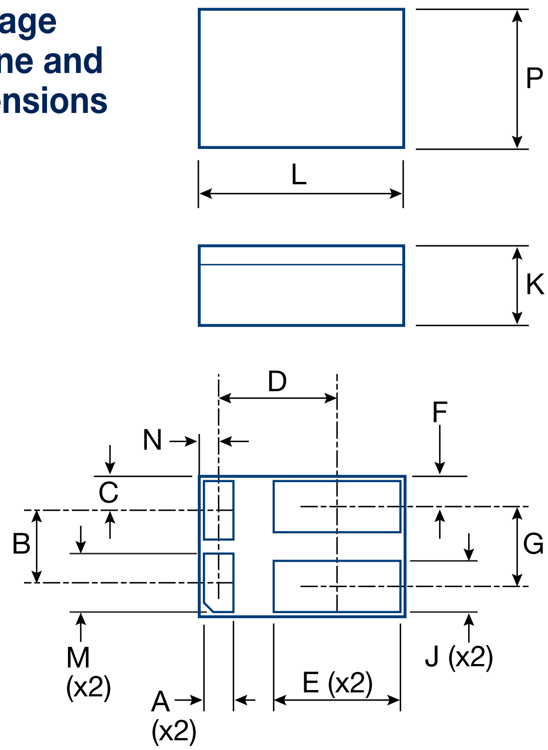



*Figure 16. Transient Thermal Impedance, Junction to Case*

## Package Outline and Dimensions

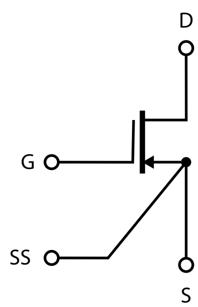



| Symbol | IN | | MM | |
|---|---|---|---|---|
| | NOM | REF | NOM | REF |
| A | 0.32 | | 0.81 | |
| B | 0.078 | | 1.98 | |
| C | | 0.036 | | 0.91 |
| D | 0.127 | | 3.23 | |
| E | 0.137 | | 3.48 | |
| F | | 0.032 | | 0.81 |
| G | 0.087 | | 2.21 | |
| J | 0.05 | | 1.27 | |
| K | | 0.083 | | 2.11 |
| L | 0.22 | | 5.69 | |
| M | 0.063 | | 1.6 | |
| N | | 0.021 | | 0.53 |
| P | 0.15 | | 0.38 | |

**Note: All dimensions have a tolerance of ±0.005 in [±0.13 mm]**

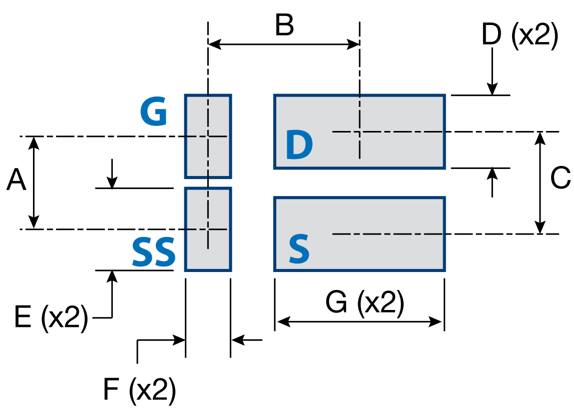
Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb

## Package Connections




**NOTE:** SS pin is connected directly to source of internal die.

## FSMD-B Footprint for Printed Circuit Board Design




| Symbol | IN | MM | Note |
|---|---|---|---|
| | NOM | NOM | |
| A | 0.078 | 1.93 | |
| B | 0.127 | 3.23 | |
| C | 0.087 | 2.21 | |
| D | 0.061 | 1.55 | |
| E | 0.069 | 1.75 | |
| F | 0.038 | 0.97 | |
| G | 0.142 | 3.61 | |

Suggested footprint:
NOM. DIM = .003 in [0.08 mm] swell on average

## Notes

Note 1. Never exceed the absolute maximum $V_{DS}$ of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum $V_{GS}$ of the device otherwise permanent damage/destruction may result. We recommend a $V_{GS}$ of 5 V for optimum operation across life and radiation.

Note 3. $R_{\theta JA}$ measured with FSMD-B package mounted to double-sided PCB, 0.063” thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 5. Guaranteed by design/device construction. Not tested.

Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current ($I_{const}$) is provided to the Gate of the DUT during the time that the ground switch ($G_S$) is OFF ($t_{off}$). The DUT is switched ON and OFF using ground-sensed switch $G_S$. The gate current is adjusted to yield the desired charge per unit time ($I_{const}$ · time per division) on the measuring oscilloscope. The $G_S$ pulse drive ON time ($t_{on}$)is adjusted for the desired observability of the gate-source voltage ($V_{GS}$) waveform. The maximum duty cycle of the ground switch ($t_{off}$/$t_{on}$) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 $V_{DC}$.

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