

Features

- Low $R_{DS(on)}$
- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
 - SEE immunity for LET of 83.2 MeV/(mg/cm²) in Si with V_{DS} up to 83% of rated Breakdown
- Low Dose Rate at 100 mRad/sec
 - Maintains Pre-Rad specification
- Neutron
 - Maintains Pre-Rad specification for up to 4×10^{13} Neutrons/cm²



FBG30N04CC

Rad-Hard eGaN® HEMT 300 V, 4 A, 370 mΩ Surface Mount (FSMD-C)

Description

EPC Space FSMD-C series of eGaN® power switching HEMTs have been specifically designed for critical applications in the high reliability or commercial satellite space environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

Application

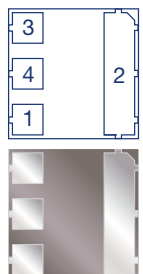
- Commercial Satellite EPS & Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	42.75	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	9.22	

I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	SS	Source Sense
4	S	Source



Absolute Maximum Rating ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	300	V
I_D	Continuous Drain Current I_D @ $V_{GS} = 5\text{ V}$, $T_C = 25^\circ\text{C}$, $R_{\theta JA} < 62^\circ\text{C/W}$	4	A
I_{DM}	Single-Pulse Drain Current $t_{pulse} \leq 80\ \mu\text{s}$	12	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{sol}	Package Mounting Surface Temperature	260	°C
ESD	ESD Class	1A(ΔA)	
Weight	Device Weight	0.113	g

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	$V_G = 0\text{ V}$	300			V
Drain to Source Leakage	I_{DSS}	$V_{DS} = 300\text{ V}$ $V_{GS} = 0\text{ V}$		10	100	μA
Gate to Source Forward Leakage	I_{GSSF}	$V_{GS} = 6\text{ V}$		250	600	
Gate to Source Reverse Leakage	I_{GSSR}	$V_{GS} = -4\text{ V}$		20	100	
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 0.6\text{ mA}$	0.8	1.2	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T$	$V_{DS} = V_{GS}, I_D = 0.6\text{ mA}$		0.5		$\text{mV}/^\circ\text{C}$
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$I_D = 4\text{ A}, V_{GS} = 5\text{ V}$		210	370	$\text{m}\Omega$
Source to Drain Forward Voltage	V_{SD}	$I_S = 0.5\text{ A}, V_G = 0\text{ V}$		1.75	3	V

Dynamic Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	$f = 1\text{ MHz}, V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$		380	400	pF
Output Capacitance	C_{OSS}			48	80	
Reverse transfer Capacitance	C_{RSS}			2	4	
Gate Resistance (Note 5)	R_G	$f = 1\text{ MHz}, V_{DS} = V_{GS} = 0\text{ V}$		0.4		Ω
Total Gate Charge (Note 6)	Q_G	$I_D = 4\text{ A}, V_{GS} = 5\text{ V}, V_{DS} = 150\text{ V}$		1.6	3	nC
Gate to Drain Charge (Note 6)	Q_{GD}	$I_D = 4\text{ A}, V_{GS} = 5\text{ V}, V_{DS} = 150\text{ V}$		1.1	1.7	
Gate to Source Charge (Note 6)	Q_{GS}	$I_D = 4\text{ A}, V_{GS} = 5\text{ V}, V_{DS} = 150\text{ V}$		0.9	2	
Output Charge (Note 5)	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 150\text{ V}$		40		
Source to Drain Recovery Charge (Note 5)	Q_{RR}	$I_D = 4\text{ A}, V_{DS} = 150\text{ V}$		<1		

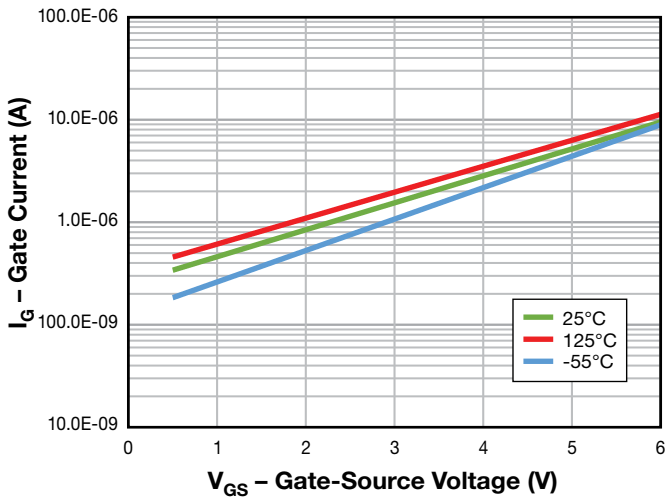


Figure 1: Typical Output Characteristics at 25°C

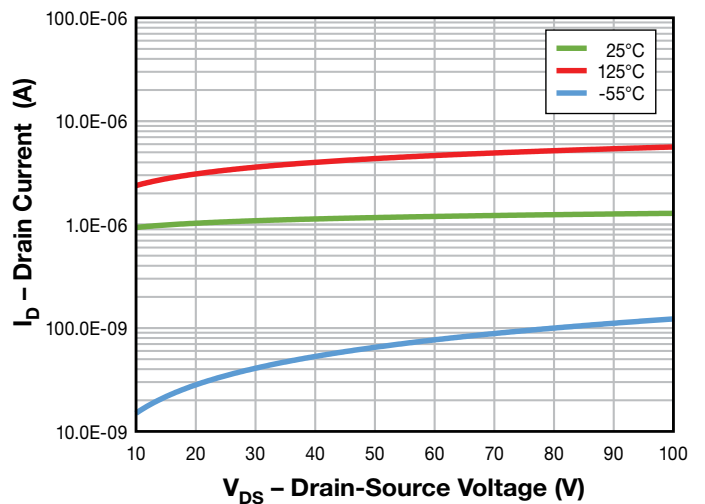


Figure 2: Typical Output Characteristics at 125°C

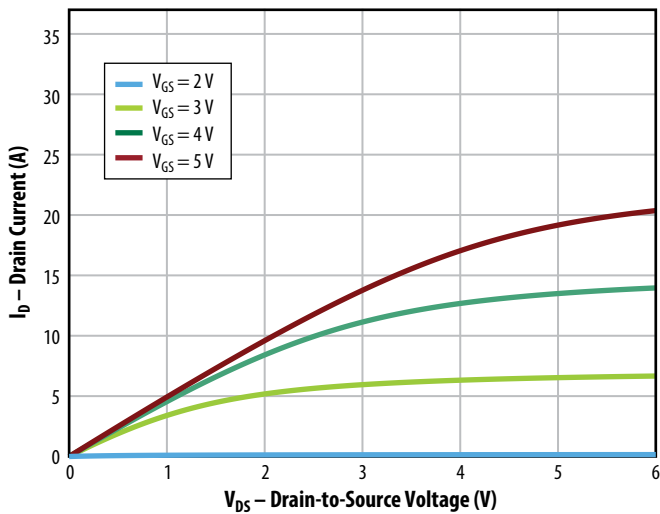


Figure 3: Typical Output Characteristics at 25°C

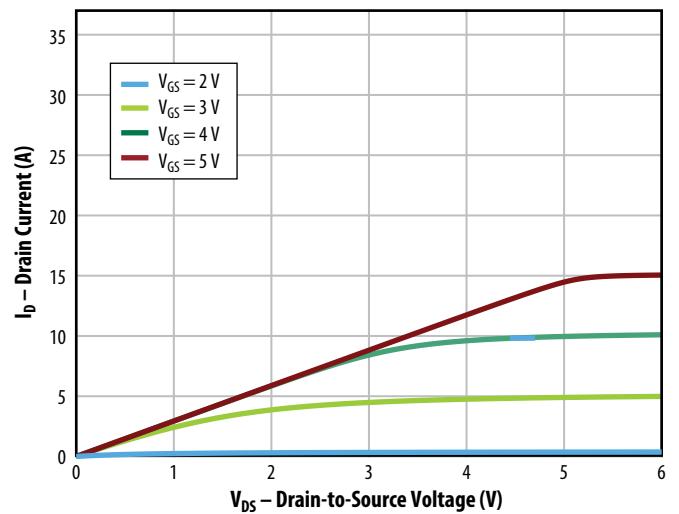


Figure 4: Typical Output Characteristics at 125°C

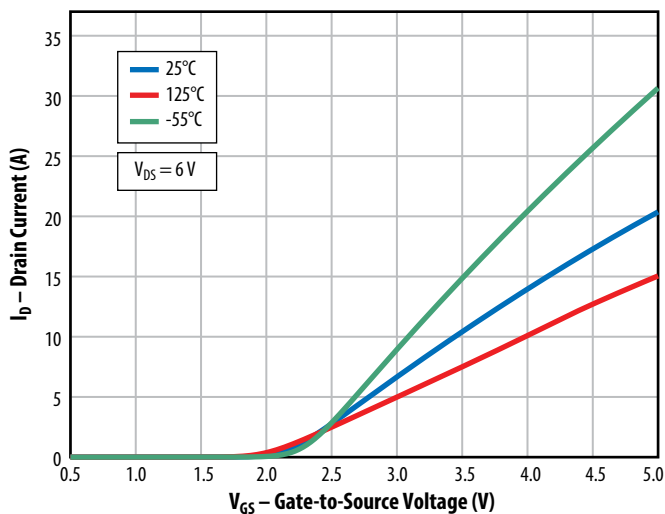


Figure 5: Typical Transfer Characteristics

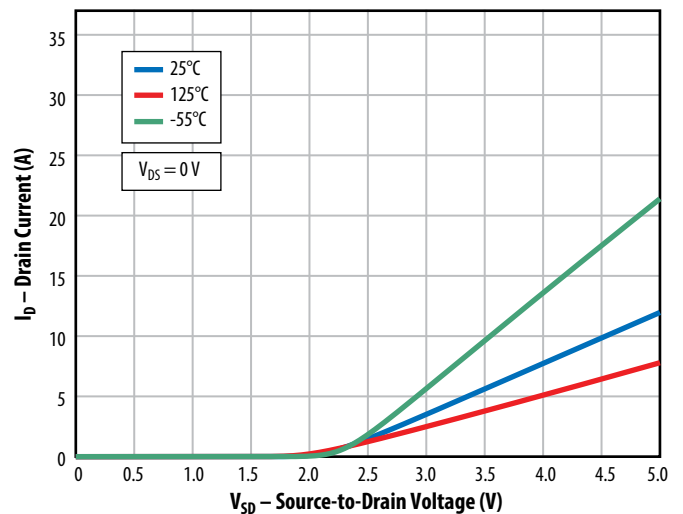


Figure 6: Reverse Drain-Source Characteristics

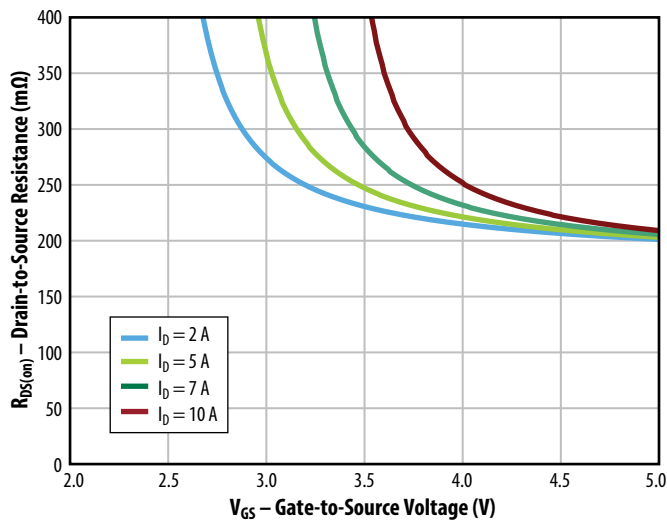


Figure 7: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

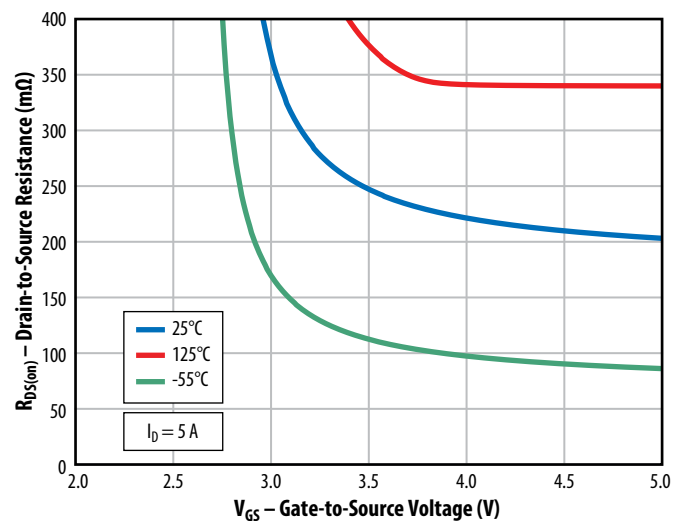


Figure 8: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

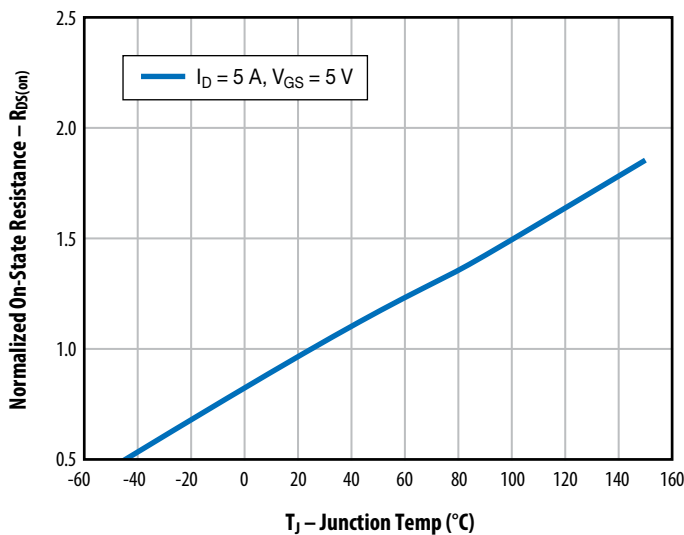


Figure 9: Normalized On-State Resistance vs. Temp.

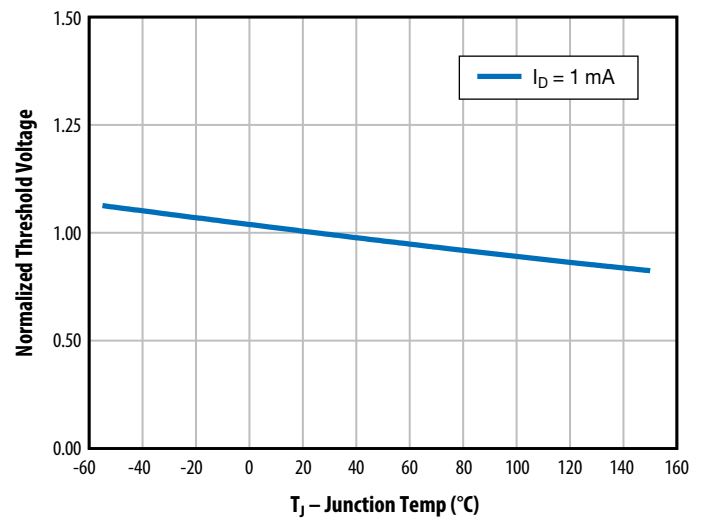


Figure 10: Normalized Gate Threshold Voltage vs. Temp.

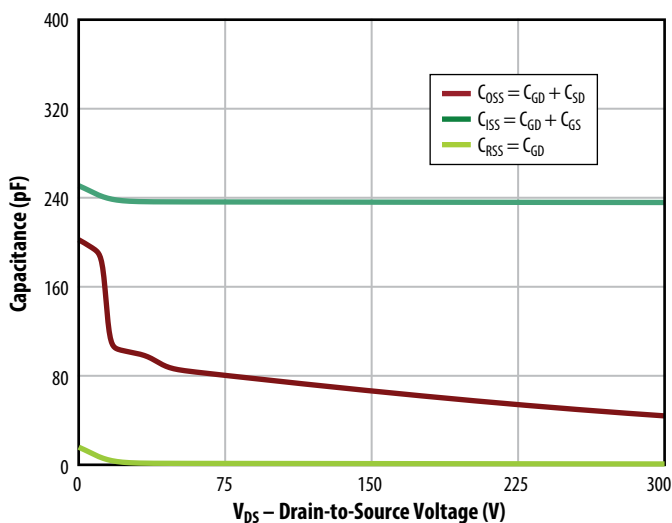


Figure 11: Typical Capacitance

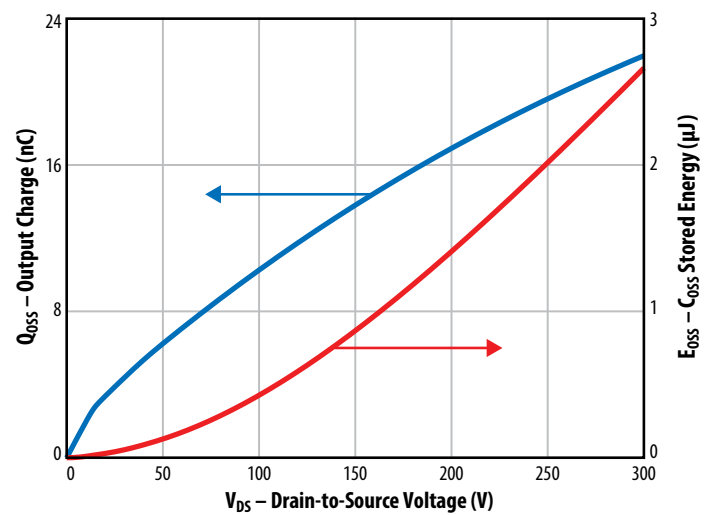


Figure 12: Typical Output Charge and C_{OSS} Stored Energy

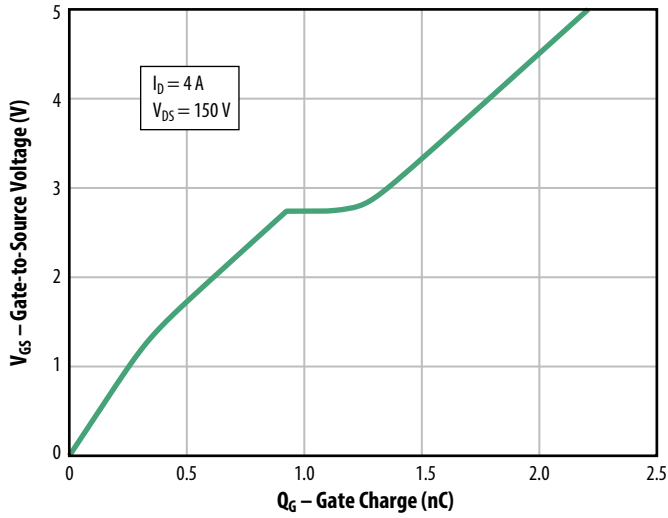


Figure 13: Typical Gate Charge

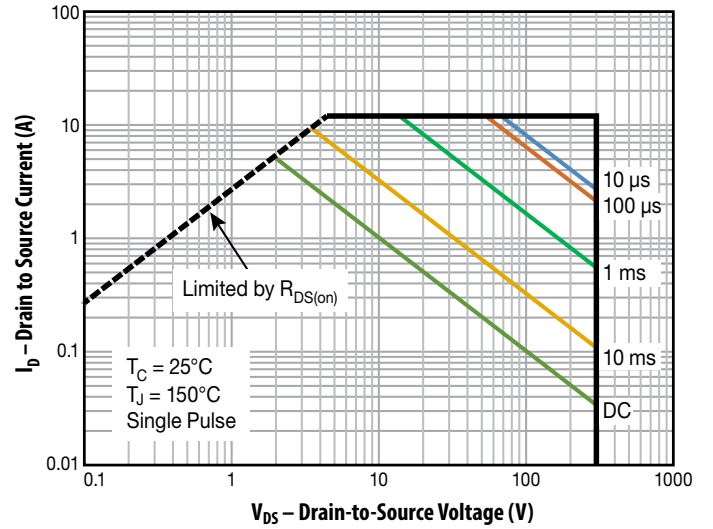


Figure 14: Safe Operating Area

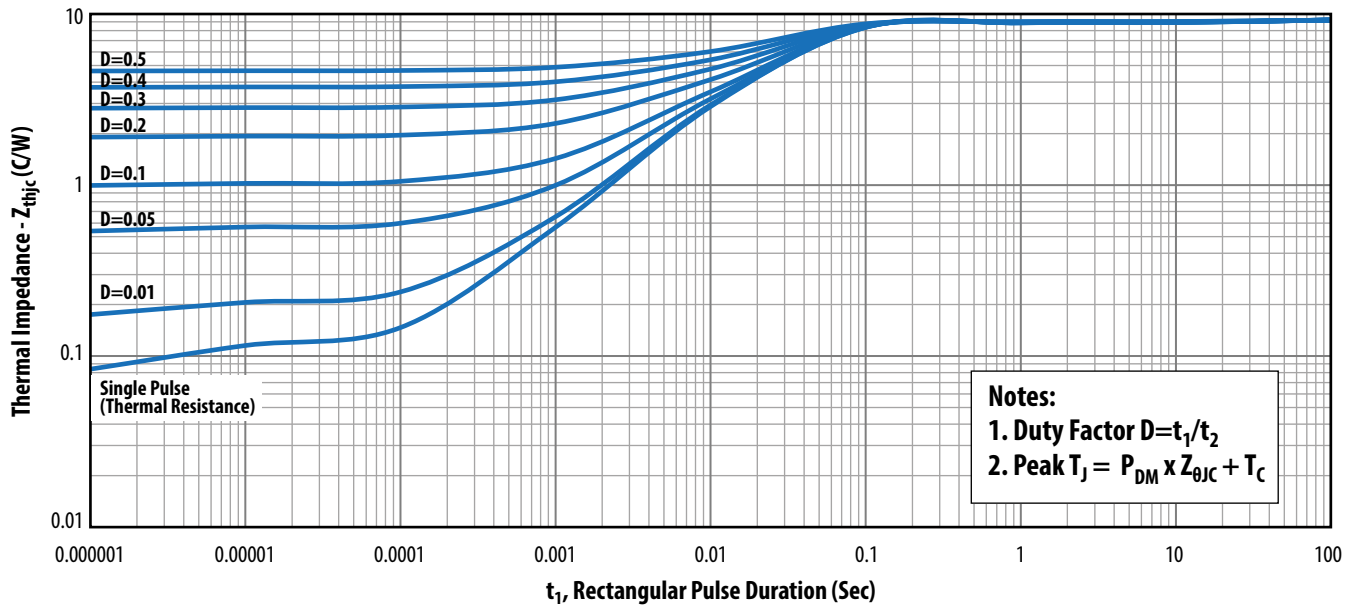
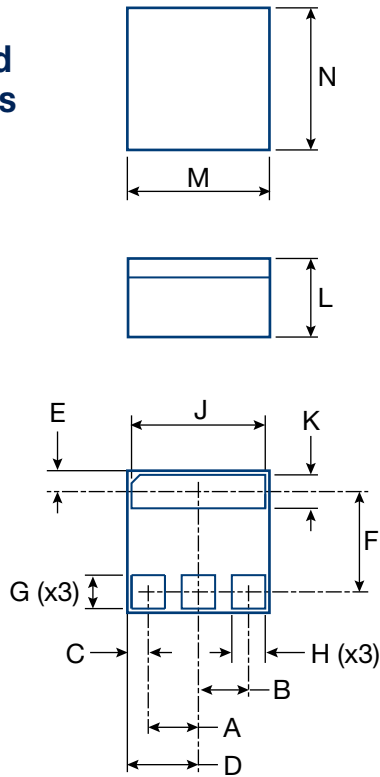


Figure 15: Thermal Impedance diagram

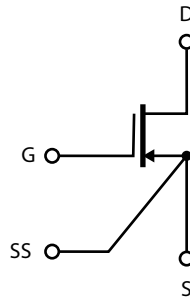
Package Outline and Dimensions



Symbol	IN		MM	
	NOM	REF	NOM	REF
A	0.06		1.52	
B	0.06		1.52	
C		0.022		0.56
D	0.085		2.16	
E		0.025		0.64
F	0.12		3.05	
G	0.04		1.02	
H	0.04		1.02	
J	0.16		4.06	
K	0.04		1.02	
L		0.083		2.11
M	0.17		4.32	
N	0.17		4.32	

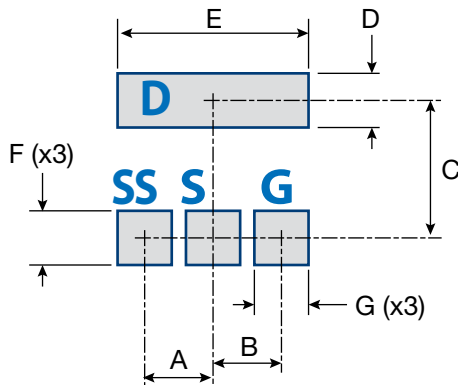
Note: All dimensions have a tolerance of ± 0.005 in [± 0.13 mm]
Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb

Package Connections



NOTE: SS pin is connected directly to source of internal die.

FSMD-C Footprint for Printed Circuit Board Design



Symbol	IN	MM	Note
	NOM	NOM	
A	0.053	1.35	
B	0.053	1.35	
C	0.106	2.69	
D	0.041	1.04	
E	0.147	3.73	
F	0.041	1.04	
G	0.041	1.04	

Suggested footprint:
NOM. DIM = .003 in [0.08 mm] swell on average

Notes

- Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5V for optimum operation across life and radiation.
- Note 3. $R_{\theta JA}$ measured with FSMD-C package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 μs and duty cycle is 1%, maximum.
- Note 5. Guaranteed by design/device construction. Not tested.
- Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S . The gate current is adjusted to yield the desired charge per unit time ($I_{const} \cdot \text{time per division}$) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} / t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC} .

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