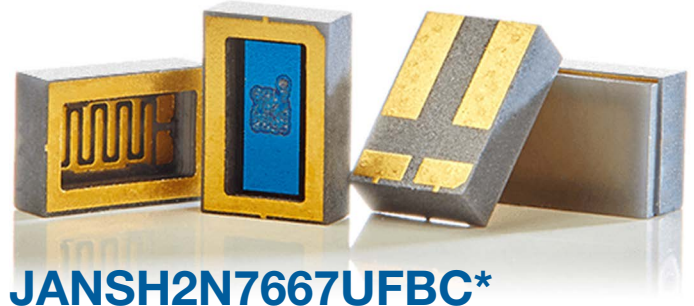


### Features

- Low  $R_{DS(on)}$
- Ultra-low  $Q_G$  For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 83.7 MeV/mg/cm<sup>2</sup> with  $V_{DS}$  up to 100% of rated Breakdown
- Neutron
  - Maintains Pre-Rad specification for up to  $4 \times 10^{15}$  Neutrons/cm<sup>2</sup>



### JANS2N7667UFBC\*

**Rad-Hard eGaN® 40 V, 30 A,  
11 mΩ Surface Mount (FSMD-B)**

### Description

EPC Space FSMD-B series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low  $R_{DS(on)}$  values. The lateral structure of the die provides for very low gate charge ( $Q_G$ ) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

\* JANS qualification pending

### Applications

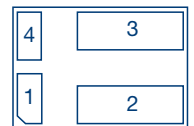
- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers

### Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	35	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	2.25	

### I/O Pin Assignment (Bottom View)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	SS	Source Sense



### Absolute Maximum Rating ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter-Conditions	Value	Units
$V_{DS}$	Drain to Source Voltage (Note 1)	40	V
$I_D$	Continuous Drain Current $I_D$ @ $V_{GS} = 4.5\text{ V}$ , $T_C = 25^\circ\text{C}$	30	A
$I_{DM}$	Single-Pulse Drain Current $t_{pulse} \leq 80\ \mu\text{s}$	120	
$V_{GS}$	Gate to Source Voltage (Note 2)	+6 / -4	V
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C
$T_{sol}$	Package Mounting Surface Temperature	260	
<b>ESD</b>	ESD Class	1A ( $\Delta A$ )	
<b>Weight</b>	Device Weight	0.135	g

Electrical Characteristics ( $T_C = 25^\circ\text{C}$  unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Minimum Drain to Source Voltage	$V_{\text{DSMIN}}$	$V_G = 0\text{ V}$	40			V
Drain to Source Leakage	$I_{\text{DSS}}$	$V_{\text{DS}} = 40\text{ V}$ $V_{\text{GS}} = 0\text{ V}$		26	400	$\mu\text{A}$
				300	1000	
Gate to Source Forward Leakage	$I_{\text{GSSF}}$	$V_{\text{GS}} = 5\text{ V}$		100	500	$\mu\text{A}$
Gate to Source Reverse Leakage	$I_{\text{GSSR}}$	$V_{\text{GS}} = -4\text{ V}$		50	400	
Gate to Source Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 5\text{ mA}$	0.8	1	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{\text{GS(th)}}/\Delta T$		$-55^\circ\text{C} < T_A < 150^\circ\text{C}$		[1.5]	
Drain to Source Resistance (Note 4)	$R_{\text{DS(on)}}$	$I_{\text{D}} = 30\text{ A}, V_{\text{GS}} = 5\text{ V}$		9	11	$\text{m}\Omega$
Source to Drain Forward Voltage	$V_{\text{SD}}$	$I_{\text{S}} = 0.5\text{ A}, V_G = 0\text{ V}$		2.5		V

Dynamic Characteristics ( $T_C = 25^\circ\text{C}$  unless otherwise noted. Typical (TYP) values are for reference only.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	$C_{\text{ISS}}$	$f = 1\text{ MHz}, V_{\text{DS}} = 20\text{ V}, V_{\text{GS}} = 0\text{ V}$		1100	1300	$\text{pF}$
Output Capacitance	$C_{\text{OSS}}$			650	900	
Reverse transfer Capacitance	$C_{\text{RSS}}$			30	60	
Gate Resistance (Note 5)	$R_G$	$f = 1\text{ MHz}, V_{\text{DS}} = V_{\text{GS}} = 0\text{ V}$		1.1		$\Omega$
Total Gate Charge (Note 6)	$Q_G$	$I_{\text{D}} = 30\text{ A}, V_{\text{GS}} = 5\text{ V}, V_{\text{DS}} = 20\text{ V}$		8.9	11.4	$\text{nC}$
Gate to Drain Charge (Note 6)	$Q_{\text{GD}}$			2.1	3.0	
Gate to Source Charge (Note 6)	$Q_{\text{GS}}$			2.3	3.1	
Output Charge (Note 5)	$Q_{\text{OSS}}$	$V_{\text{GS}} = 0\text{ V}, V_{\text{DS}} = 20\text{ V}$		22	26	
Source to Drain Recovery Charge	$Q_{\text{RR}}$	$I_{\text{D}} = 30\text{ A}, V_{\text{DS}} = 20\text{ V}$		<1		

### Radiation Characteristics

EPC Space eGaN<sup>®</sup> HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON	$V_{GS} = 5\text{ V}$
NO BIAS	$V_{DS} = V_{GS} = 0\text{ V}$
OFF	$V_{DS} = 80\% B_{VDSS}$

**Electrical Characteristics up to 1000 krad ( $T_C = 25^\circ\text{C}$  unless otherwise noted. Typical (TYP) values are for reference only.)**

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	$V_{DSMAX}$	$V_{GS} = 0\text{ V}$	40			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 5\text{ mA}$	0.8	1	2.5	
Drain to Source Leakage	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		26	400	$\mu\text{A}$
Gate to Source Forward Leakage	$I_{GSSF}$	$V_{GS} = 5\text{ V}$		100	500	
Gate to Source Reverse Leakage	$I_{GSSR}$	$V_{GS} = -4\text{ V}$		50	400	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	$I_D = 30\text{ A}, V_{GS} = 5\text{ V}$		9	11	$\text{m}\Omega$

### Typical Single Event Effect Safe Operating Area

Note: All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.

Test	Environment				$V_{DS}$ Voltage (V)	
	Ion	LET $\text{MeV}/\text{mg}/\text{cm}^2$	Range $\mu\text{m}$	Energy MeV	$V_{GS} = 0\text{ V}$	$V_{GS} = -4\text{ V}$
See SOA	Xe	50	131	1653	40	40
	Au	83.7	130	2482	40	40

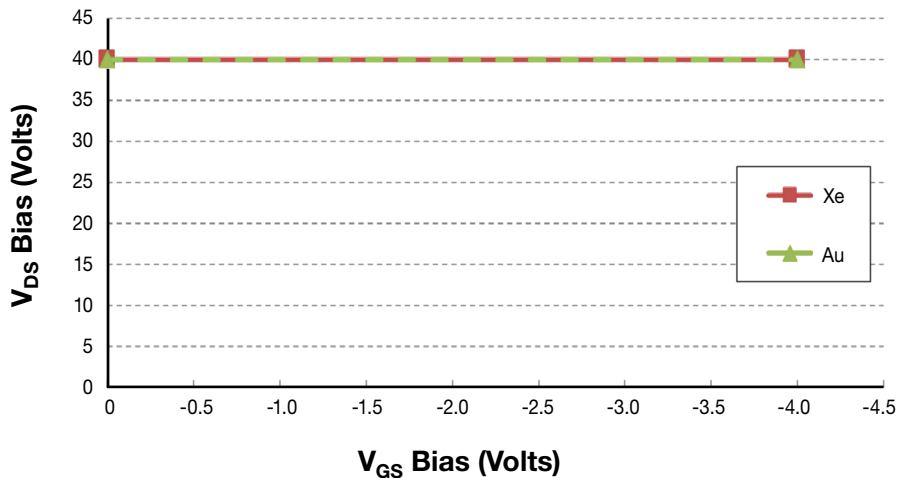


Figure 1. Typical Single Event Effect Safe Operating Area

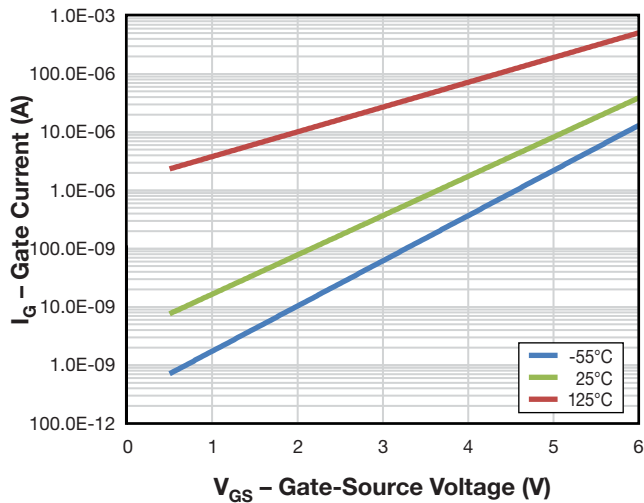


Figure 2. Typical Gate-Source Leakage Current vs. Ambient Temperature

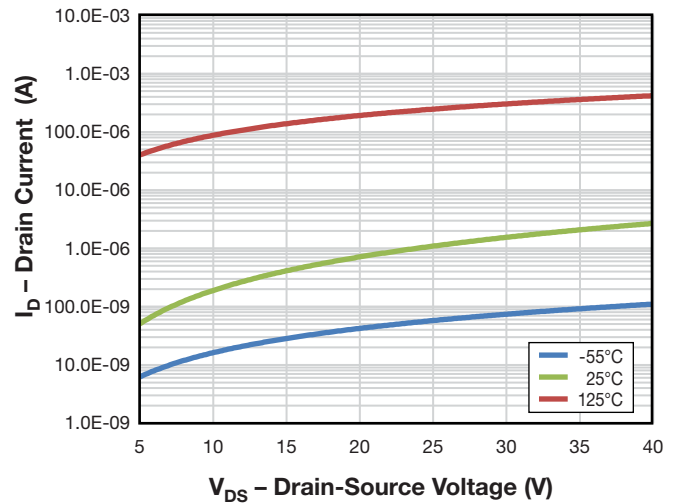


Figure 3. Typical Drain-Source Leakage Current vs. Ambient Temperature

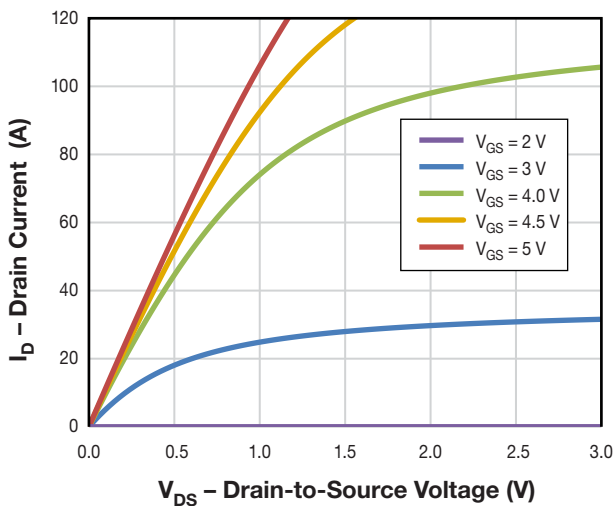


Figure 4. Typical Output Characteristics at  $25^\circ\text{C}$

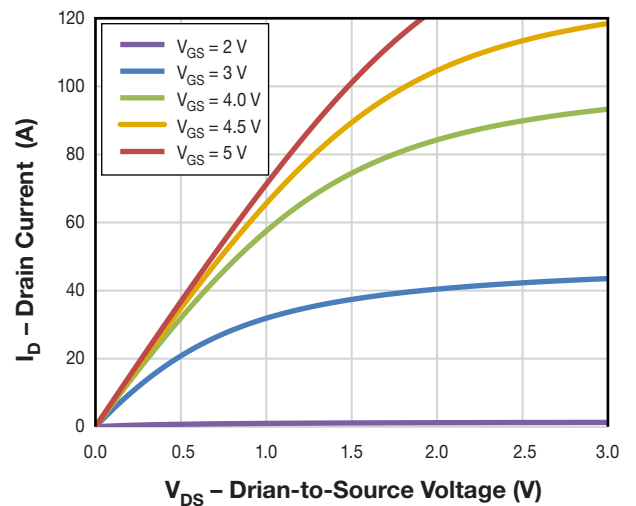


Figure 5. Typical Output Characteristics at  $125^\circ\text{C}$

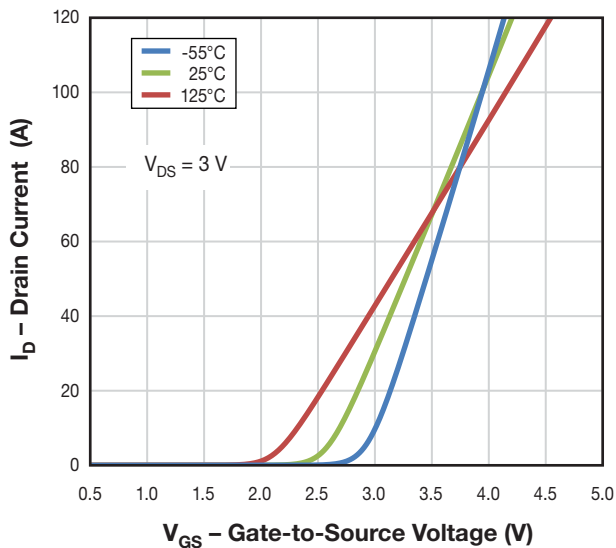


Figure 6. Typical Transfer Characteristics

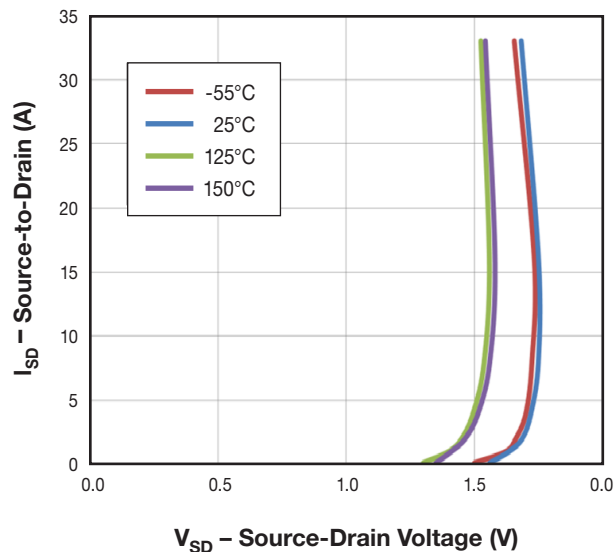


Figure 7. Reverse Drain-Source Characteristics

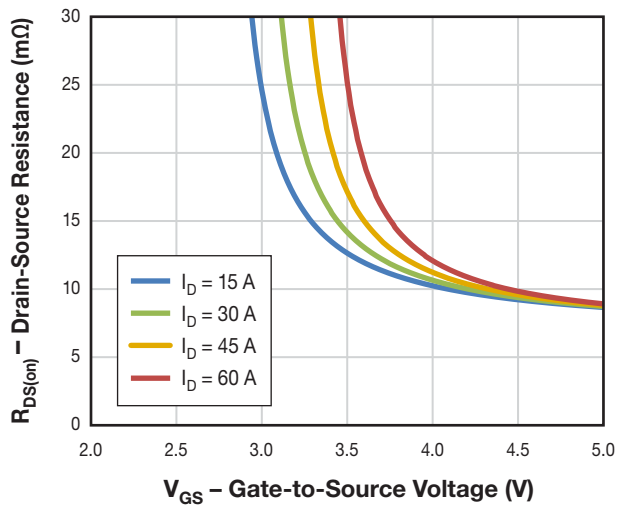


Figure 8.  $R_{DS(on)}$  vs  $V_{GS}$  for Various Drain Currents

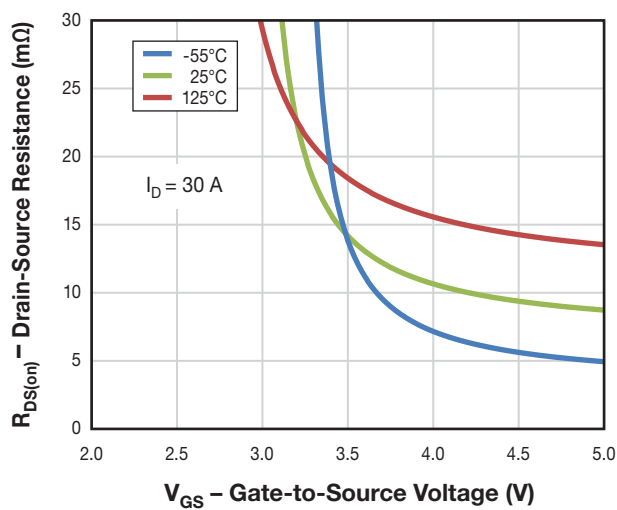


Figure 9.  $R_{DS(on)}$  vs  $V_{GS}$  for Various Temperatures

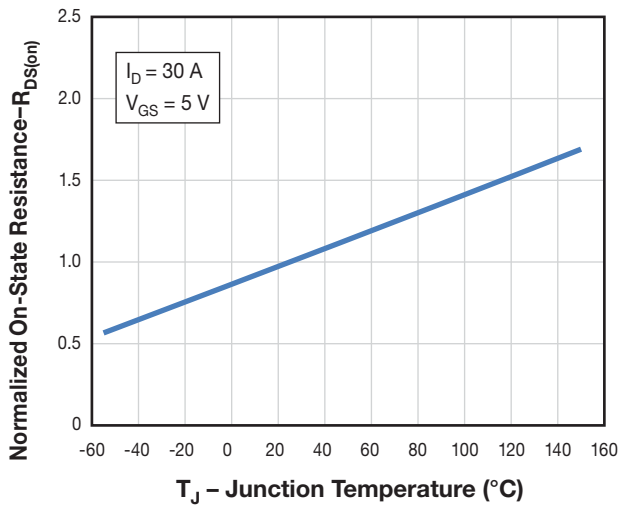


Figure 10. Normalized On-State Resistance vs. Temperature

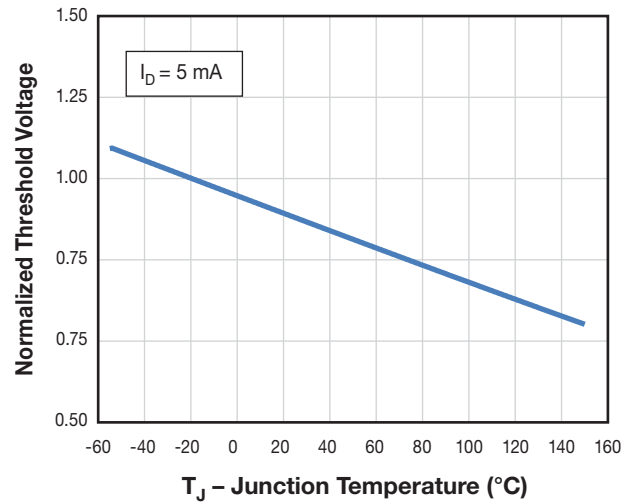


Figure 11. Normalized Threshold Voltage vs. Temperature

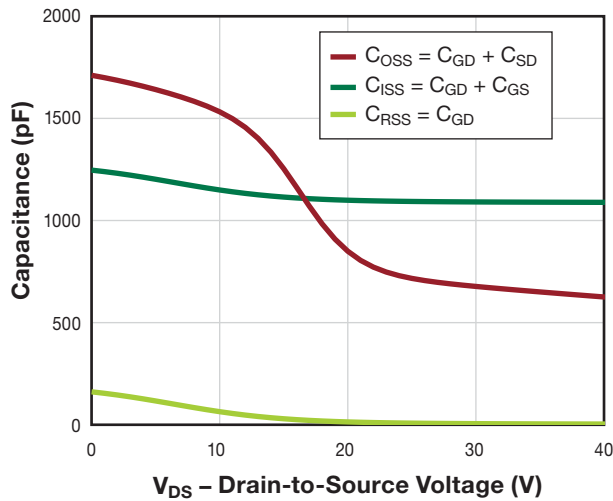


Figure 12. Typical Capacitance

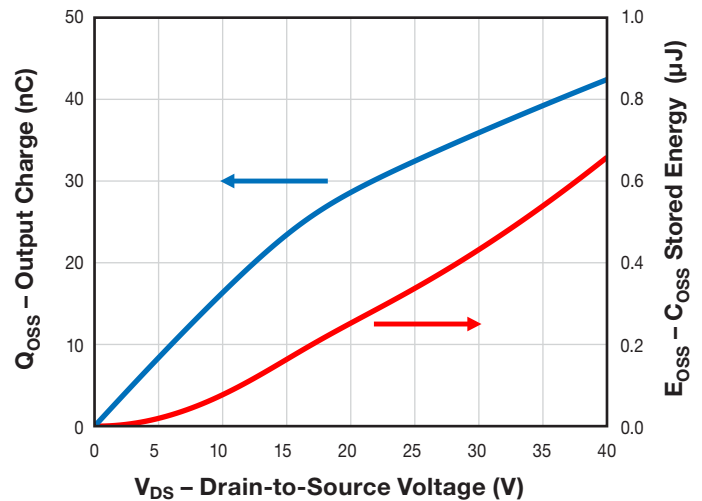


Figure 13. Typical Output Charge and  $C_{OSS}$  Stored Energy

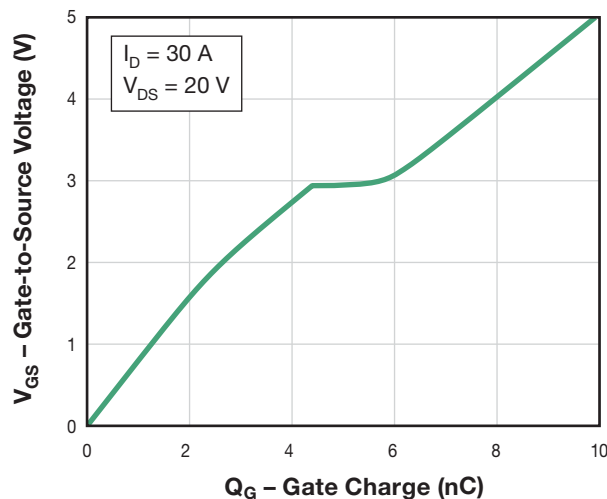


Figure 14. Typical Gate Charge

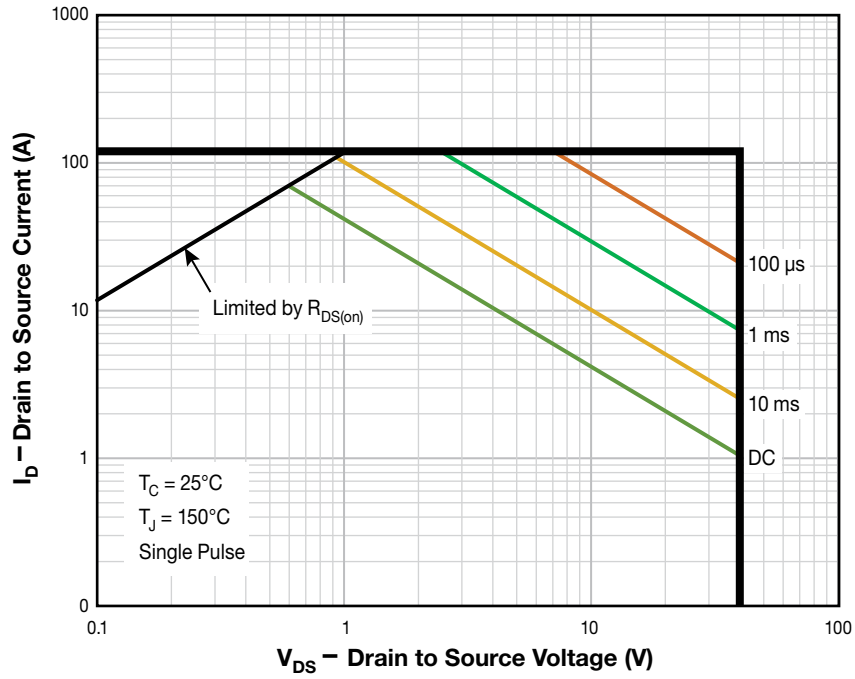


Figure 15. Safe Operating Area

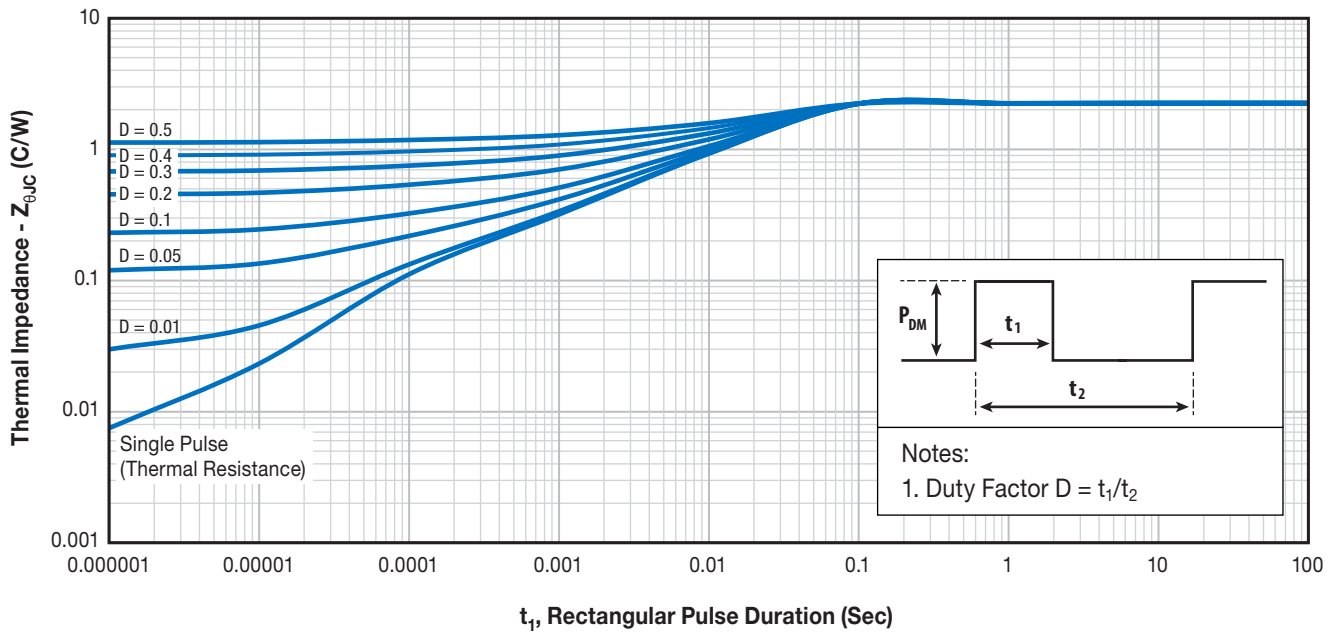
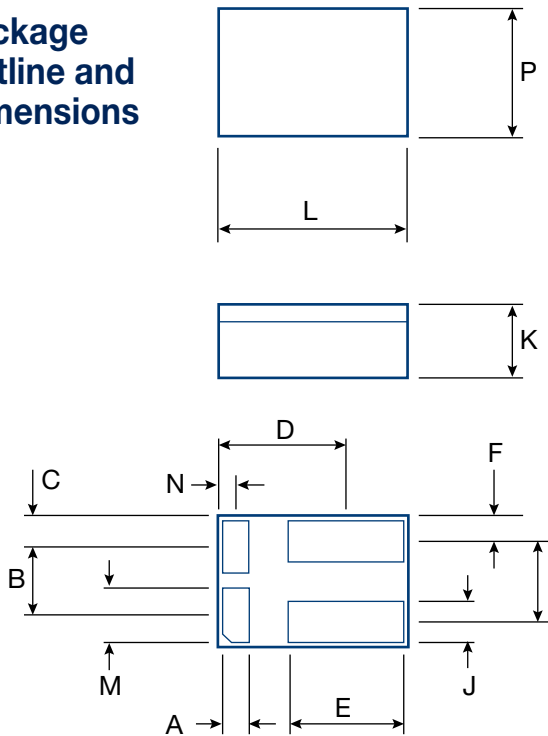


Figure 16. Transient Thermal Impedance, Junction to Case

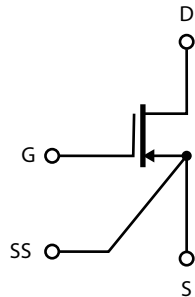
**Package Outline and Dimensions**



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
<b>A</b>	0.027	0.037	0.685	0.939	
<b>B</b>	0.073	0.083	1.854	2.108	
<b>C</b>	0.031	0.041	0.784	1.041	
<b>D</b>	0.143	0.153	3.632	3.886	
<b>E</b>	0.129	0.139	3.277	3.531	
<b>F</b>	0.027	0.037	0.686	0.940	
<b>G</b>	0.082	0.092	2.083	2.337	
<b>J</b>	0.050	0.060	1.270	1.524	
<b>K</b>	0.078	0.088	1.981	2.235	Ref. only
<b>L</b>	0.215	0.225	5.461	5.715	
<b>M</b>	0.058	0.068	1.473	1.727	
<b>N</b>	0.016	0.026	0.406	0.660	
<b>P</b>	0.145	0.155	3.683	3.937	

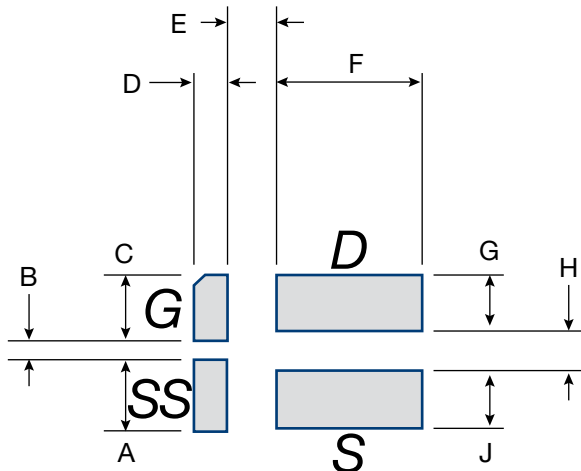
Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb.

**Package Connections**



**NOTE:** SS pin is connected directly to source of internal die.

**FSMD-B Footprint for Printed Circuit Board Design**



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
<b>A</b>	0.064	0.074	1.626	1.880	
<b>B</b>	0.010	0.020	0.254	0.508	
<b>C</b>	0.064	0.074	1.626	1.880	
<b>D</b>	0.036	0.046	0.914	1.168	
<b>E</b>	0.034	0.044	0.864	1.118	
<b>F</b>	0.135	0.145	3.429	3.683	
<b>G</b>	0.059	0.069	1.499	1.753	
<b>H</b>	0.020	0.030	0.508	0.762	
<b>J</b>	0.059	0.069	1.499	1.753	



## Notes

- Note 1. Never exceed the absolute maximum  $V_{DS}$  of the device otherwise permanent damage/destruction may result.
- Note 2. Never exceed the absolute maximum  $V_{GS}$  of the device otherwise permanent damage/destruction may result. We recommend a  $V_{GS}$  of 5 V for optimum operation across life and radiation.
- Note 3.  $R_{\theta JA}$  measured with FSMD-B package mounted to double-sided PCB, 0.063" thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.
- Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80  $\mu$ s and duty cycle is 1%, maximum.
- Note 5. Guaranteed by design/device construction. Not tested.
- Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current ( $I_{const}$ ) is provided to the Gate of the DUT during the time that the ground switch ( $G_S$ ) is OFF ( $t_{off}$ ). The DUT is switched ON and OFF using ground-sensed switch  $G_S$ . The gate current is adjusted to yield the desired charge per unit time ( $I_{const} \cdot \text{time per division}$ ) on the measuring oscilloscope. The  $G_S$  pulse drive ON time ( $t_{on}$ ) is adjusted for the desired observability of the gate-source voltage ( $V_{GS}$ ) waveform. The maximum duty cycle of the ground switch ( $t_{off}/t_{on}$ ) should be set to 1% maximum. Please note that all gate-related signals are referenced to the "Source Sense" pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5  $V_{DC}$ .

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