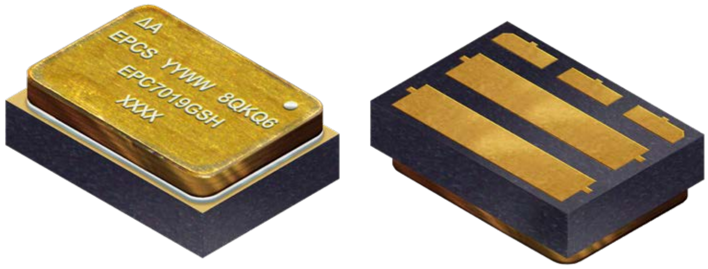
Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package Dual Gate
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity up to LET of 84 MeV/mg/cm^2 with V_{DS} up to 100% of rated Breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 4 x 10^{15} Neutrons/cm^2

Applications

- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities



JANSH2N7678UFGC*

Rad-Hard eGaN® 40 V, 90 A,
4.5 mΩ Surface Mount (FSMD-G)

Description

EPC Space FSMD-G series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

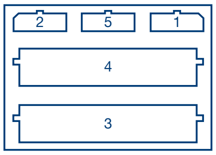
* JANS qualification pending

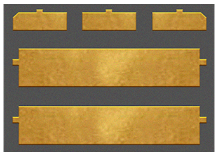
Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	48	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.55	

I/O Pin Assignment *(Bottom View)*

Pin	Symbol	Description
1	G	Gate
2	G	Gate
3	D	Drain
4	S	Source
5	SS	Source Sense





Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous Drain Current ID @ V_{GS} = 5 V	90	A
I_{DM}	Single-Pulse Drain Current t_{pulse} = 300 µs	477	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{SOL}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1B (ΔB)	
Weight	Device Weight	0.170	g

Static Characteristics *(Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Drain to Source Voltage	B_{VDSS}	V_{GS} = 0 V		40			V
Drain to Source Leakage	I_{DSS}	V_{DS} = 40 V	T_C = 25°C		0.001	0.4	mA
		V_{GS} = 0 V	T_C = 125°C		0.01	0.8	
Gate to Source Forward Leakage	I_{GSSF}	V_{GS} = 5 V	T_C = 25°C		0.05	0.5	
Gate to Source Forward Leakage#		V_{GS} = 5 V	T_C = 125°C		0.2	1	
Gate to Source Reverse Leakage	I_{GSSR}	V_{GS} = -4 V	T_C = 25°C		0.05	0.5	
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 18 mA	T_C = 25°C	0.8	1.4	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}$		-55°C < T_A < 150°C		|2.0|		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	V_{GS} = 5 V, I_D = 50 A	T_C = 25°C		3.7	4.5	mΩ
Source to Drain Forward Voltage	V_{SD}	I_S = 0.5 A, V_G = 0 V	T_C = 25°C		2	3	V

Dynamic Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 20 V, V_{GS} = 0 V		2830		pF
Reverse transfer Capacitance	C_{RSS}			35		
Output Capacitance	C_{OSS}			1660		
Effective Output Capacitance, Energy Related	$C_{OSS(ER)}$	V_{DS} = 0 to 20 V, V_{GS} = 0 V		2130		
Effective Output Capacitance, Time Related	$C_{OSS(TR)}$			2540		
Total Gate Charge (Note 5)	Q_G	V_{DS} = 0 to 20 V, V_{GS} = 0 V, I_D = 50 A		22		nC
Gate to Source Charge (Note 5)	Q_{GS}	V_{DS} = 20 V, I_D = 50 A		9.1		
Gate to Drain Charge (Note 5)	Q_{GD}			3.4		
Output Charge (Note 5)	Q_{OSS}	V_{DS} = 20 V, V_{GS} = 0 V		51		
Source to Drain Recovery Charge (Note 6)	Q_{RR}			0		

Radiation Characteristics

EPC Space eGaN® HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON | V_{GS} = 5 V
NO BIAS | V_{DS} = V_{GS} = 0 V
OFF | V_{DS} = 80% B_{VDSS}

Electrical Characteristics up to 1000 krads *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	V_{GS} = 0 V	40			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 18 mA	0.8	1.4	2.5	
Drain to Source Leakage	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		0.001	0.4	mA
Gate to Source Forward Leakage	I_{GSSF}	V_{GS} = 5 V		0.05	0.5	
Gate to Source Reverse Leakage	I_{GSSR}	V_{GS} = -4 V		0.05	0.5	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	I_D = 50 A, V_{GS} = 5 V		3.7	4.5	mΩ

Typical Single Event Effect Safe Operating Area

Note: All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.

Test	Environment				V_{DS} Voltage (V)	
See SOA	Ion	LET MeV/mg/cm²	Range µm	Energy MeV	V_{GS} = 0 V	V_{GS} = -4V
	Xe	50	131	1653	40	40
	Au	84	130	2482	40	40

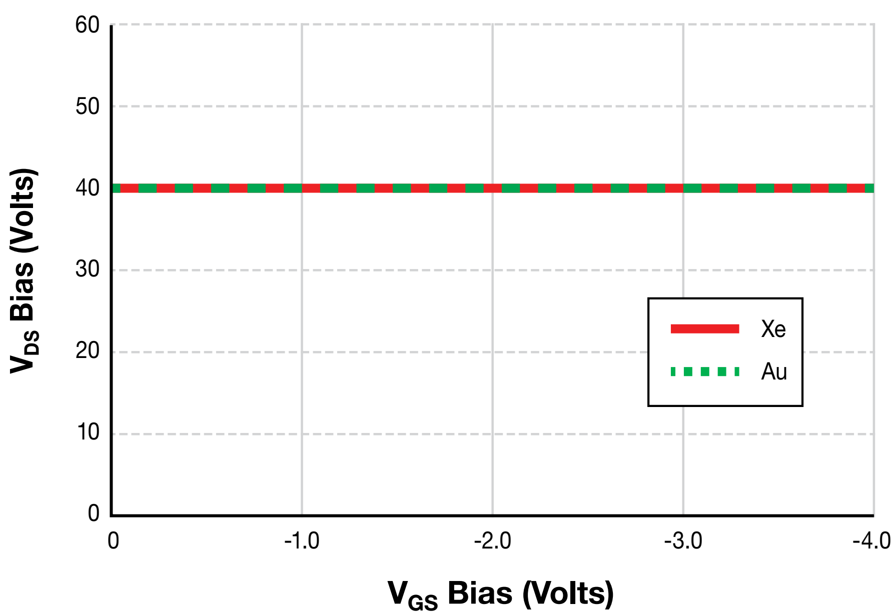


Figure 1: Typical Single Event Effect Safe Operating Area

Figure 2: Typical Output Characteristics at 25°C

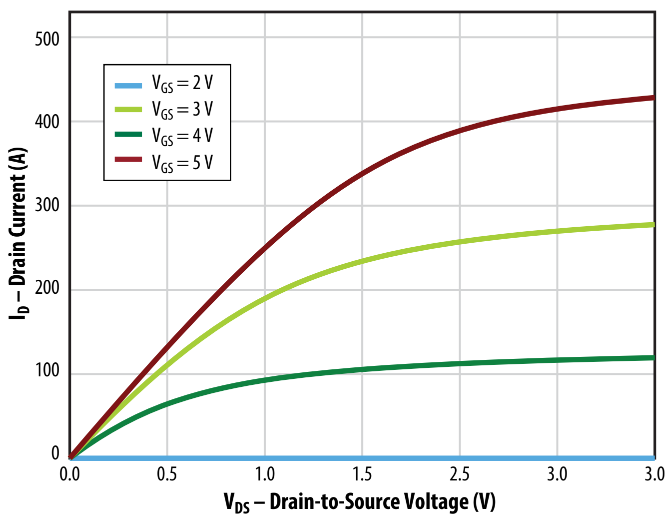


Figure 3: Typical Output Characteristics at 125°C

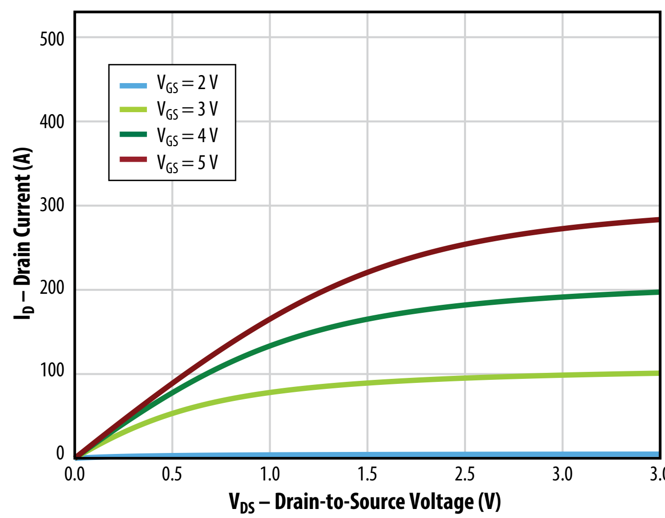


Figure 4: Typical Transfer Characteristics

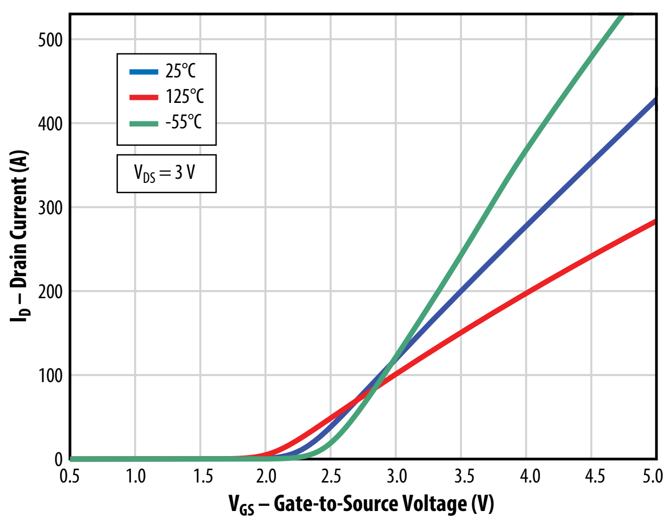


Figure 5: Reverse Drain-Source Characteristics

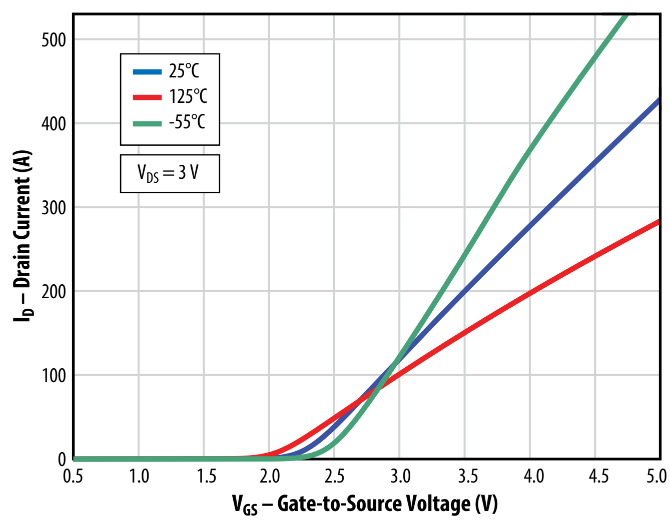


Figure 6: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

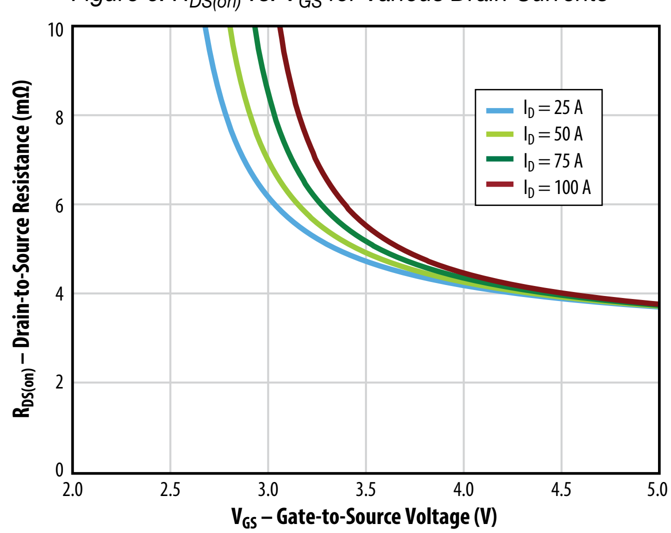


Figure 7: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

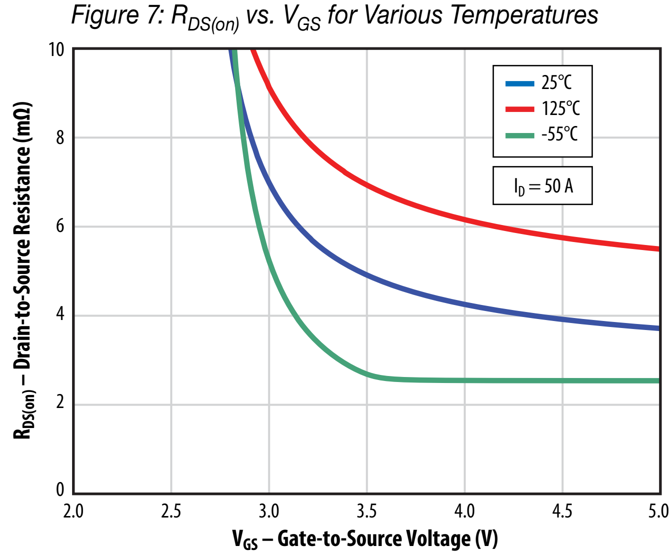


Figure 8: Normalized On-State Resistance vs. Temp.

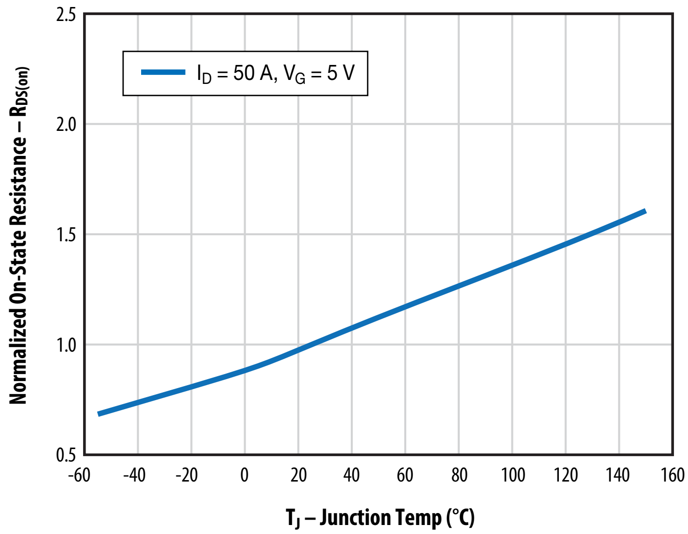


Figure 9: Normalized On-State Resistance vs. Temp.

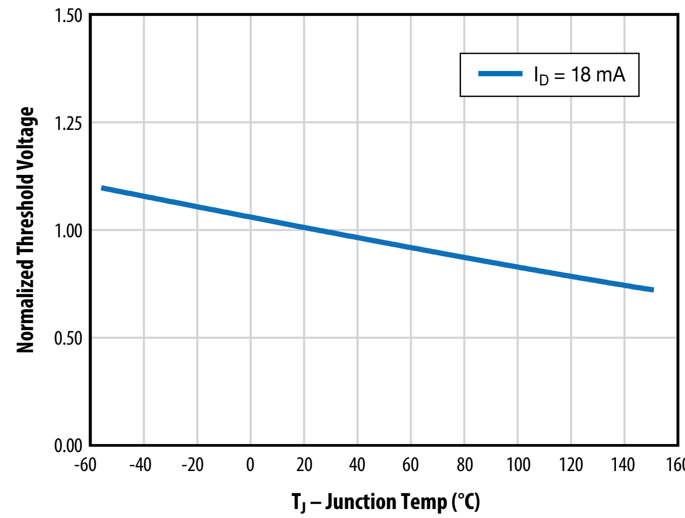


Figure 10: Typical Capacitance

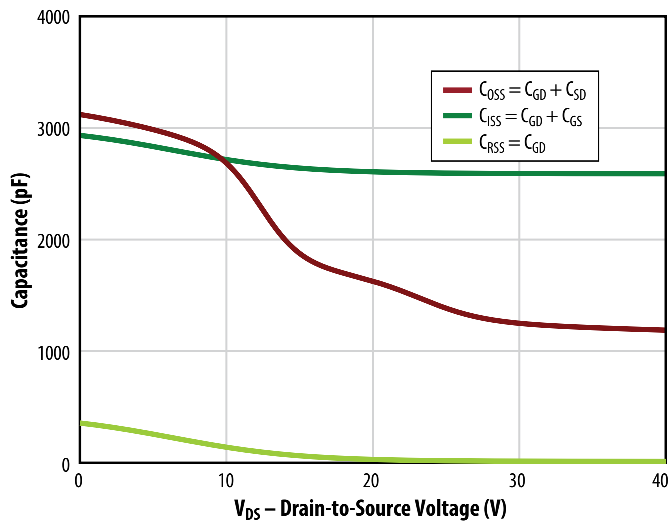


Figure 11: Typical Output Charge and C_{OSS} Stored Energy

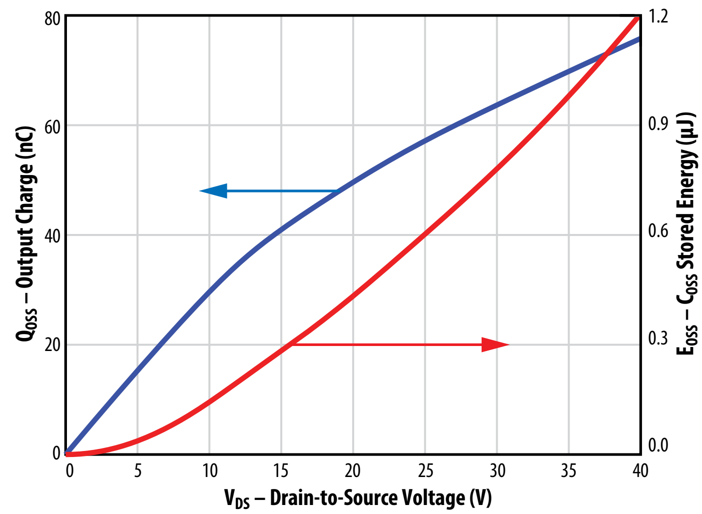
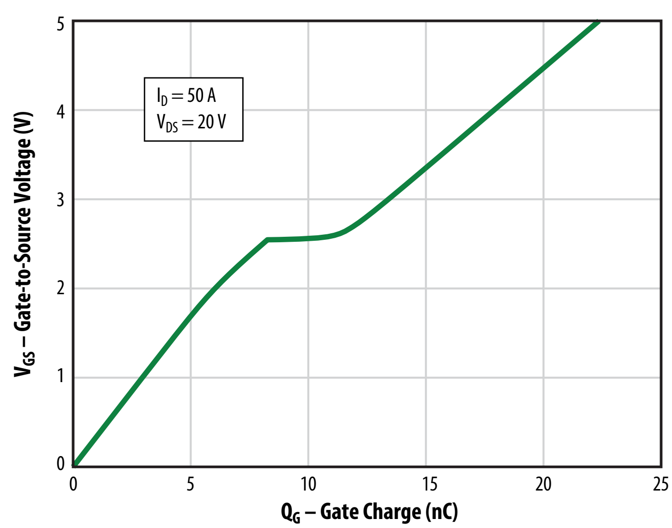
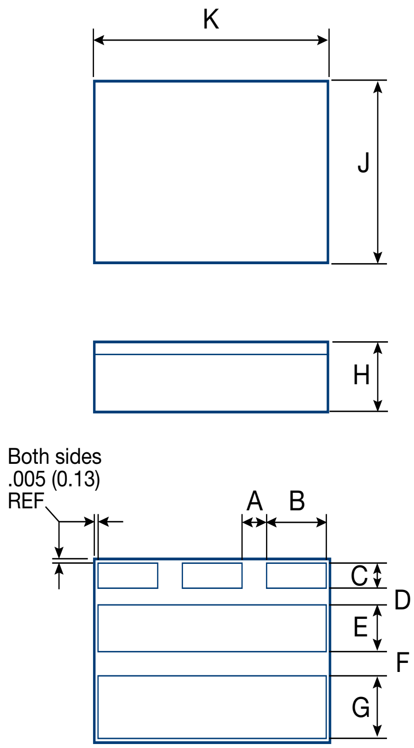


Figure 10: Typical Capacitance

Figure 12: Typical Gate Charge



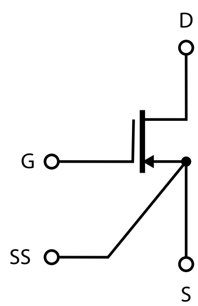
Package Outline and Dimensions



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
A (2x)	0.028	0.038	0.711	0.965	
B (3x)	0.075	0.085	1.905	2.159	
C (3x)	0.025	0.035	0.635	0.889	
D	0.015	0.025	0.381	0.635	
E	0.051	0.061	1.295	1.549	
F	0.024	0.034	0.61	0.864	
G	0.07	0.08	1.778	2.032	
H	0.078	0.088	1.981	2.235	
J	0.215	0.225	5.461	5.715	
K	0.311	0.321	7.899	8.153	

Standard Terminal Pad finish is a solder alloy of 63%Pb 37%Sn

Package Connections



NOTE: SS pin is connected directly to source of internal die.

Notes

Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5 V for optimum operation across life and radiation.

Note 3. $R_{\theta JA}$ measured with FSMD-G package mounted to double-sided PCB, 0.063” thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 5. Guaranteed by design/device construction. Not tested.

Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

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