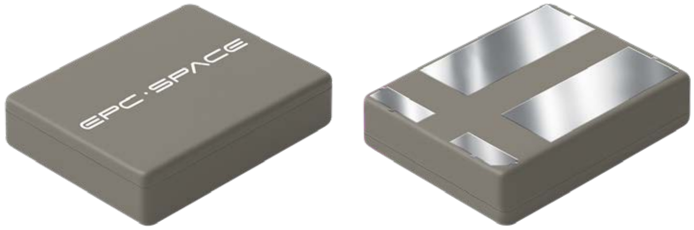
Features

- Ultra-low Q_G For High Efficiency
- Logic Level
- Light Weight
- Compact Hermetic Package Dual Gate
- Source Sense Pin
- Total Ionizing Dose LDR Immune
- Total Ionizing Dose HDR Immune
- Single Event Effect (SEE) Hardened
  - SEE immunity for LET of 83.2 MeV/(mg/cm^2) in Si with V_{DS} up to 250 V
- Neutron
  - Maintains Pre-Rad specification for up to 4 x 10^{15} Neutrons/cm^2

Applications

- Satellite and Avionics
- Deep Space Probes
- High Speed Rad-Hard DC-DC Conversion
- Rad-Hard Motor Controllers
- Nuclear Facilities



JANSH2N7684UFMC*

Rad-Hard eGaN® 300 V, 50 A, 26 mΩ Surface Mount (FSMD-M)

Description

EPC Space FSMD-M series of eGaN® power switching HEMTs have been specifically designed for critical applications in Space and other the high reliability environments. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

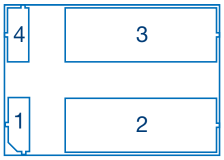
*JANS qualification pending.

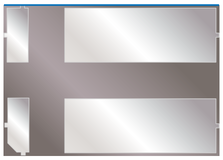
Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 3)	35	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.94	

I/O Pin Assignment *(Bottom View)*

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source
4	SS	Source Sense





Absolute Maximum Rating *(T_C = 25°C unless otherwise noted)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	Drain to Source Voltage (Note 1)	300	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	360	
I_D	Continuous Drain Current ID @ V_{GS} = 5 V	50	A
I_{DM}	Single-Pulse Drain Current t_{pulse} = 300 µs	150	
V_{GS}	Gate to Source Voltage (Note 2)	+6 / -4	V
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_{SOL}	Package Mounting Surface Temperature	260	
ESD	ESD Class	1B (ΔB)	
Weight	Device Weight	0.190	g

Static Characteristics *(Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	V_{GS} = 0 V		300			V
Drain to Source Leakage	I_{DSS}	V_{DS} = 300 V, V_{GS} = 0 V	T_C = 25°C		11	400	µA
		V_{DS} = 300 V, V_{GS} = 0 V	T_C = 125°C		22	800	
Gate to Source Forward Leakage	I_{GSSF}	V_{GS} = 6 V	T_C = 25°C		0.4	600	
Gate to Source Forward Leakage		V_{GS} = 6 V	T_C = 125°C		1	1000	
Gate to Source Reverse Leakage	I_{GSSR}	V_{GS} = -4 V	T_C = 25°C		5	0.5	
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 18 mA	T_C = 25°C	0.8	1. 5	2.5	V
Gate to Source Threshold Voltage Temperature Coefficient	$\Delta V_{GS(th)}$		-55°C < T_A < 150°C		|2.0|		mV/°C
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	V_{GS} = 5 V, I_D = 50 A	T_C = 25°C		15	26	mΩ
Source to Drain Forward Voltage	V_{SD}	I_S = 0.5 A, V_G = 0 V	T_C = 25°C		1.7	3	V

Dynamic Characteristics *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Input Capacitance	C_{ISS}	V_{DS} = 150 V, V_{GS} = 0 V		1155		pF
Reverse transfer Capacitance	C_{RSS}			10		
Output Capacitance	C_{OSS}			235		
Effective Output Capacitance, Energy Related (Note 5)	$C_{OSS(ER)}$	V_{DS} = 0 to 150 V, V_{GS} = 0 V		970		
Effective Output Capacitance, Time Related (Note 5)	$C_{OSS(TR)}$			1250		
Total Gate Charge (Note 6)	Q_G	V_{DS} = 150 V, V_{GS} = 5 V, I_D = 50 A		25	30	nC
Gate to Source Charge (Note 6)	Q_{GS}			8	10	
Gate to Drain Charge (Note 6)	Q_{GD}			4	7	
Output Charge (Note 5)	Q_{OSS}	V_{DS} = 150 V, V_{GS} = 0 V		147		
Source to Drain Recovery Charge (Note 5)	Q_{RR}			0		

Radiation Characteristics

EPC Space eGaN® HEMTs are tested according to MIL-STD-750 Method 1019 for total ionizing dose validation. Every manufacturing lot is tested for total ionizing dose of 1 Mrad of Gamma radiation exposure with an in-situ bias for the following conditions:

ON | V_{GS} = 5 V
NO BIAS | V_{DS} = V_{GS} = 0 V
OFF | V_{DS} = 80% B_{VDSS}

Electrical Characteristics up to 1000 krads *(T_C = 25°C unless otherwise noted. Typical (TYP) values are for reference only.)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Maximum Drain to Source Voltage	V_{DSMAX}	V_{GS} = 0 V	300			V
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 18 mA	0.8	1.5	2.5	
Drain to Source Leakage	I_{DSS}	V_{DS} = 300 V, V_{GS} = 0 V		11	400	µA
Gate to Source Forward Leakage	I_{GSS}	V_{GS} = 6 V		0.4	600	
Gate to Source Reverse Leakage		V_{GS} = -4 V		5	0.5	
Drain to Source Resistance (Note 4)	$R_{DS(on)}$	I_D = 50 A, V_{GS} = 5 V		15	35	mΩ

Typical Single Event Effect Safe Operating Area

Note : All Radiation Single Event Effects testing are performed in heavy ion environments such as the K-500 Cyclotron at Texas A&M.

Test	Environment				V_{DS} Voltage (V)	
See SOA	Ion	LET MeV(mg/cm²) in Si (+/-5%)	Range µm (+/- 7.5%)	Energy MeV (+/-10%)	V_{GS} = 0 V	V_{GS} = -4V
	Xe	63.6	71.3	963	300	300
	Au	83.2	121.4	2256	250	250

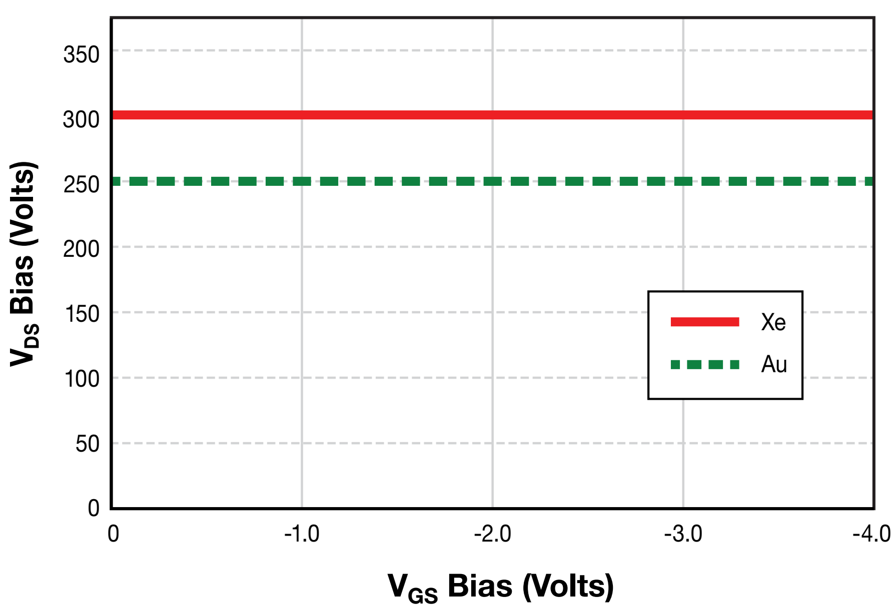


Figure 1: Typical Single Event Effect Safe Operating Area

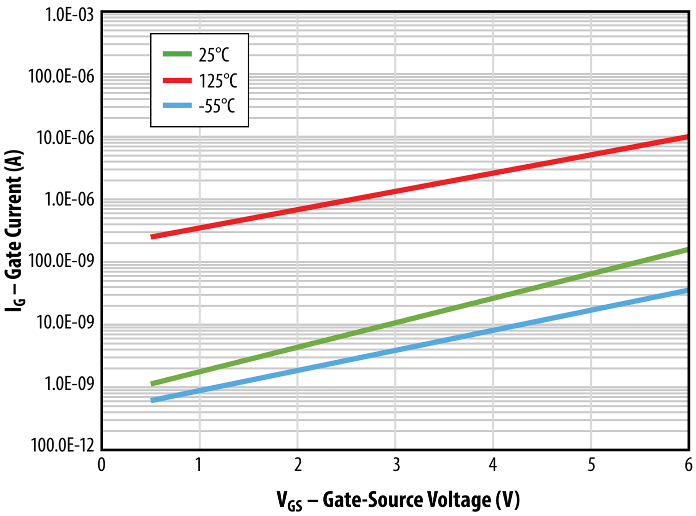


Figure 2: Typical Gate-Source Leakage Current vs. Ambient Temperature

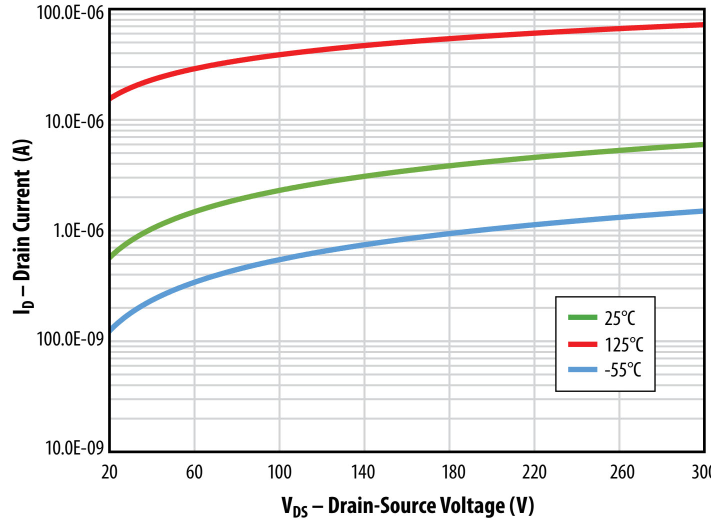


Figure 3: Typical Drain-Source Leakage Current vs. Ambient Temperature

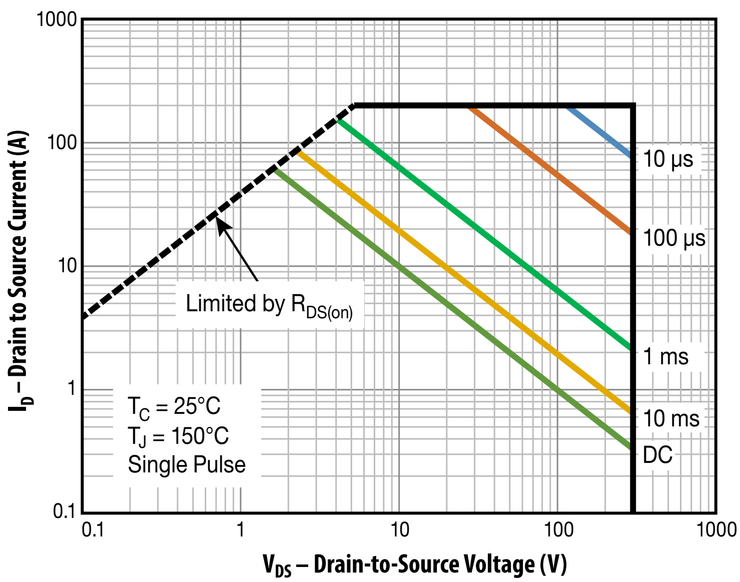


Figure 4: Safe Operating Area

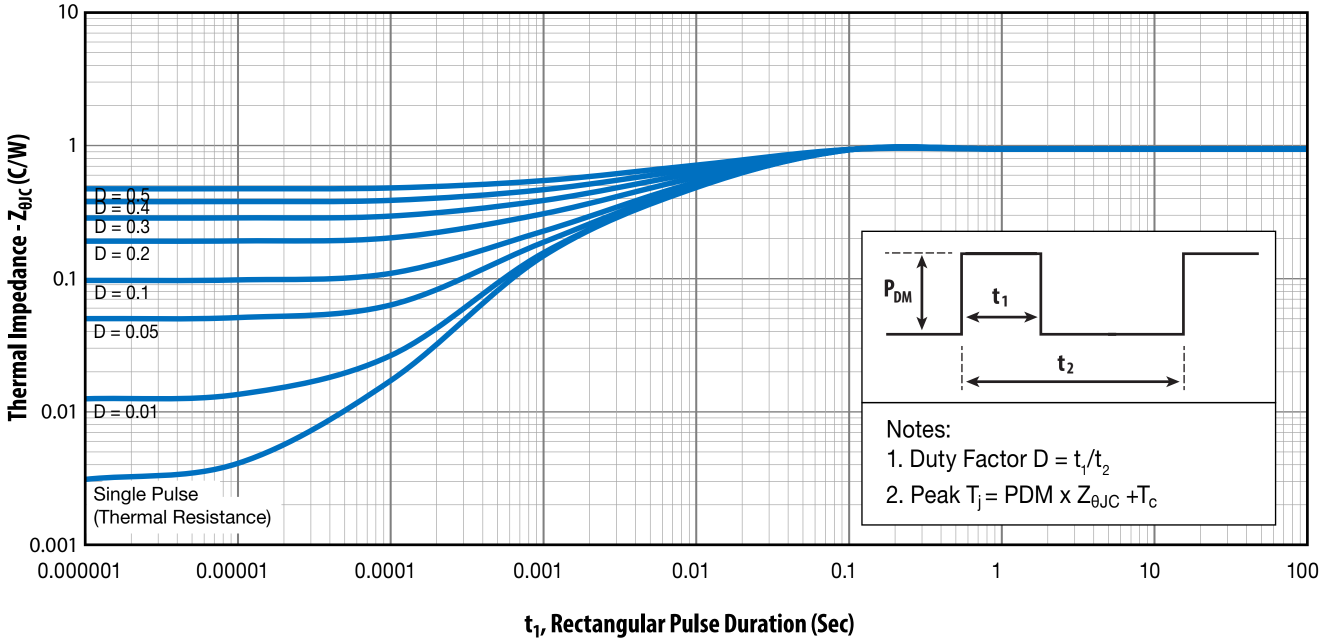
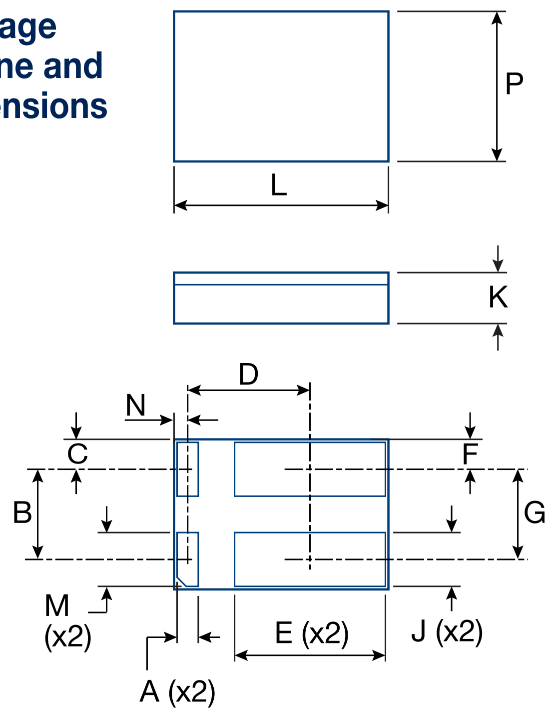


Figure 5: Thermal Impedance diagram

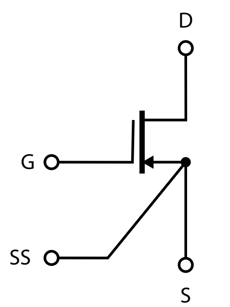
Package Outline and Dimensions



Symbol	IN		MM	
	NOM	REF	NOM	REF
A	0.035		0.89	
B	0.149		3.78	
C		0.049		1.24
D	0.202		5.13	
E	0.249		6.32	
F	0.059	0.049		1.24
G	0.154		3.68	
J	0.089		2.26	
K		0.083		2.11
L	0.354		8.99	
M	0.089		2.26	
N		0.022		0.56
P	0.249		6.32	

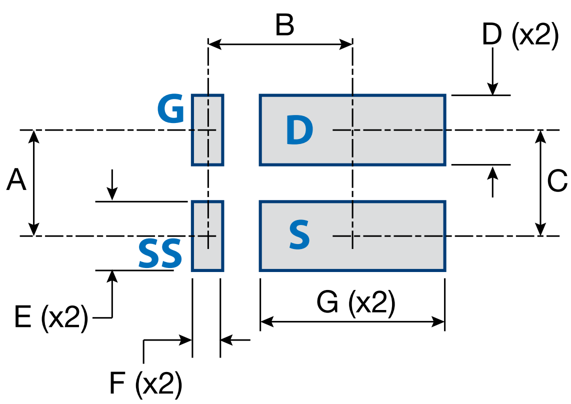
Note: All dimensions have a tolerance of ±0.005 in [±0.13 mm]
Standard Terminal Pad finish is a solder alloy of 63%Sn 37%Pb

Package Connections



NOTE: SS pin is connected directly to source of internal die.

FSMD-M Footprint for Printed Circuit Board Design



Symbol	IN	MM	Note
	NOM	NOM	
A	0.149	3.78	
B	0.202	5.13	
C	0.149	3.78	
D	0.095	2.41	
E	0.095	2.41	
F	0.041	1.04	
G	0.255	6.48	

Suggested footprint:
NOM. DIM = .003 in [0.08 mm] swell on average

Notes

Note 1. Never exceed the absolute maximum V_{DS} of the device otherwise permanent damage/destruction may result.

Note 2. Never exceed the absolute maximum V_{GS} of the device otherwise permanent damage/destruction may result. We recommend a V_{GS} of 5V for optimum operation across life and radiation.

Note 3. $R_{\theta JA}$ measured with FSMD-M package mounted to double-sided PCB, 0.063” thickness with 1.0 square inches of copper area on the top (mounting side) and a flood etch (3 square inches) on the bottom side.

Note 4. Measured using four wire (Kelvin) sensing and pulse measurement techniques. Measurement pulse width is 80 µs and duty cycle is 1%, maximum.

Note 5. Guaranteed by design/device construction. Not tested.

Note 6. The gate charge parameters are measured based on the MIL-STD-750.3471 Condition B. A high speed constant gate current (I_{const}) is provided to the Gate of the DUT during the time that the ground switch (G_S) is OFF (t_{off}). The DUT is switched ON and OFF using ground-sensed switch G_S. The gate current is adjusted to yield the desired charge per unit time (I_{const} · time per division) on the measuring oscilloscope. The G_S pulse drive ON time (t_{on}) is adjusted for the desired observability of the gate-source voltage (V_{GS}) waveform. The maximum duty cycle of the ground switch (t_{off} /t_{on}) should be set to 1% maximum. Please note that all gate-related signals are referenced to the “Source Sense” pin on the package. At all times during the measurement, the maximum gate-source voltage is clamped to 5 V_{DC}.

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