EPC Space Model Report: EPC7014

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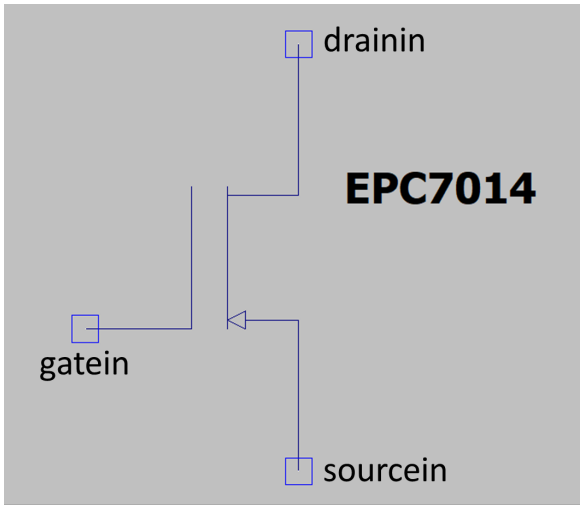
2. Symbol

2.1. Summary

The model package includes a generic symbol as shown below.

Figure 2.1-1 Generic SPICE symbol.



The symbol generates a netlist entry with pin order D G S. No additional parameters are necessary, but users can pass their own values for the parameters defined in this model report.

3. Model

3.1. Summary

The EPC Space model contains the sub-circuit shown below.

Figure 3.1-1 EPC Space Model.

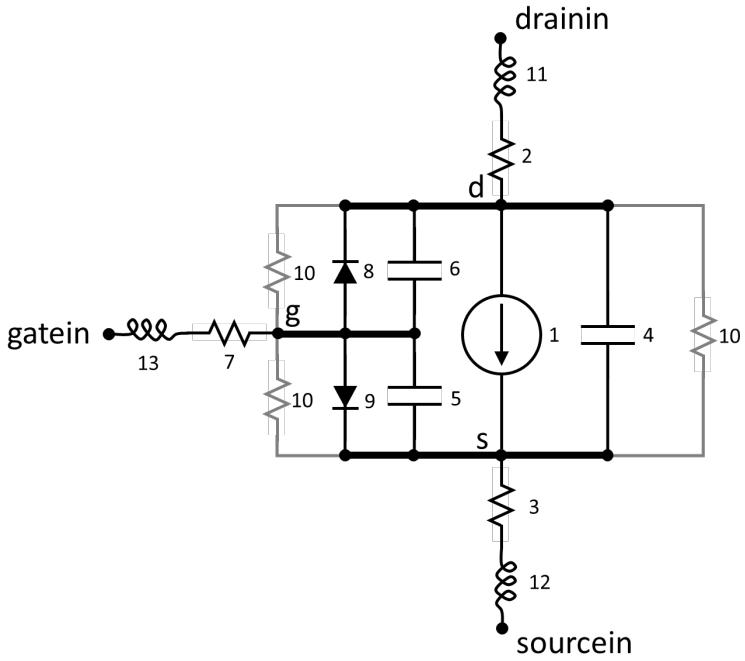


Table 3.1-1. Sub-circuit component definitions.

#	Name	Description
1	I(Vg, Vd, Vs)	Channel
2	Rd	Drain-side parasitic resistance
3	Rs	Source-side parasitic resistance
4	Cds(Vd, Vs)	Drain-source capacitance
5	Cgs(Vg, Vs)	Gate-source capacitance
6	Cgd(Vg, Vd)	Gate-drain capacitance
7	Rg	Gate resistance
8	I(Vg, Vd)	Gate-drain leakage
9	I(Vg, Vs)	Gate-source leakage
10	Rconv	Convergence aid (~GΩ)
11	Ld	Drain-side inductance
12	Ls	Source-side inductance
13	Lg	Gate-side inductance

The known limitations of the model are as follows:

- Based on measurements between 25 and 150 °C.
- Gate leakages are not based on data and are modeled as unidirectional.

4. EPC7014 Model

4.1. Model Parameters

Model parameters are listed below along with their default (typical) values and suggested ranges.

Table 4.1-1. Model Parameters.

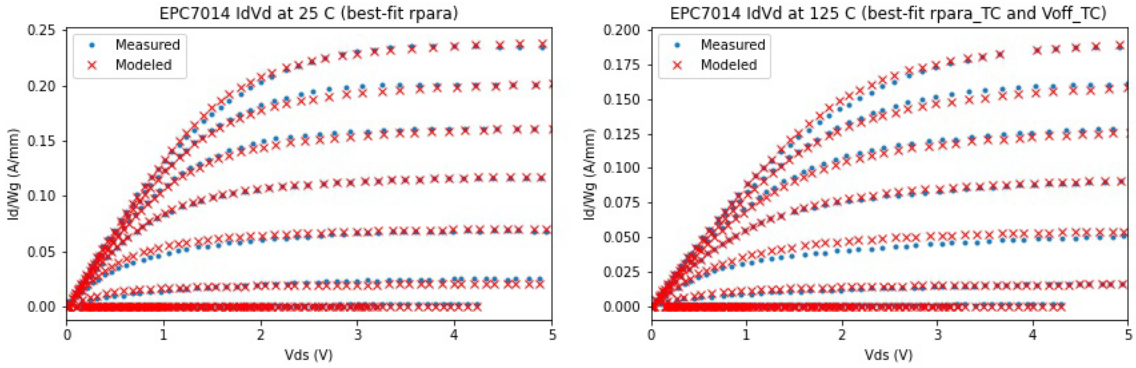
Parameter	Units	Description	Typical	Fast	Slow	Source of F/S param.
aWg	mm	Gate width	27			
A1	S/mm	Normalized peak transconductance	0.1425	0.1453	0.1399	Observed variation
Voff	V	Threshold voltage	2.33	1.50	3.20	DS limits
rpara	Ω	Total chip scale parasitic resistance	0.224	0.20	0.249	Observed variation
Vdsat	V	*Vds* where output curves transition to saturation	0.315			
ua	V^{-1}	Coefficient of mobility degradation with vertical electric field	0.144	0.151	0.138	Observed variation
Vgshape	V	Overdrive voltage effect on *Vdsat*	4.02			
k3	V	Sub-threshold swing parameter	0.09			
rpara_s_factor	(none)	Fraction of the chip scale parasitic resistance on the source side	0.215			
rg_value	Ω	Gate Resistance	12.6			
pack_indd	H	Drain-side inductance	3.55E-09			
pack_inds	H	Source-side inductance	3.55E-09			
pack_indg	H	Gate-side inductance	4.40E-09			
pack_rd	Ω	Additional drain-side resistance from packaging	5.65E-02			
pack_rs	Ω	Additional source-side resistance from packaging	5.65E-02			
pack_rg	Ω	Additional gate-side resistance from packaging	0.0			
A1_TC	K^{-1}	Temp.-co. of *A1*	1.70E-03	1.93E-03	1.47E-03	Observed variation
Voff_TC	K^{-1}	Temp.-co. of *Voff*	8.93E-04	1.93E-03	-1.41E-04	Observed variation
Vdsat_TC	K^{-1}	Temp.-co. of *Vdsat*	3.59E-02	6.85E-02	3.19E-03	Observed variation
rpara_TC	K^{-1}	Temp.-co. of *rpara*	-7.58E-03	-8.16E-03	-7.00E-03	Observed variation
Vgshape_TC	K^{-1}	Temp.-co. of *Vgshape*	-2.88E-03	-3.51E-03	-2.25E-03	Observed variation
cgs0	F/mm	Voltage-independent gate-source capacitance	5.25E-13	5.11E-13	5.39E-13	Observed variation
cgs_a	F/mm	Amplitude of voltage-dependent gate-source capacitance	3.27E-13			
cgs_av	V	Location in voltage space of voltage-	2.098	1.3	3	DS Limits

Parameter	Units	Description	Typical	Fast	Slow	Source of F/S param.
		dependent capacitance				
cgs_aw	V	Transition width of voltage-dependent capacitance	0.29317			
cgd0	F/mm	Voltage-independent gate-drain capacitance	1.94E-15			
cgd_a	F/mm	Amplitude of voltage-dependent gate-drain capacitance	1.18E-13			
cgd_av	V	Location in voltage space of voltage-dependent capacitance	-5			
cgd_aw	V	Transition width of voltage-dependent capacitance	4.314			
cgd_b	F/mm	Amplitude of voltage-dependent gate-drain capacitance	7.79E-15			
cgd_bv	V	Location in voltage space of voltage-dependent capacitance	-17.26			
cgd_bw	V	Transition width of voltage-dependent capacitance	15.29			
csd0	F/mm	Voltage-independent drain-source capacitance	2.61E-13			
csd_a	F/mm	Amplitude of voltage-dependent drain-source capacitance	4.78E-13			
csd_av	V	Location in voltage space of voltage-dependent capacitance	-13.35			
csd_aw	V	Transition width of voltage-dependent capacitance	1.2066			
csd_b	F/mm	Amplitude of voltage-dependent drain-source capacitance	7.59E-13			
csd_bv	V	Location in voltage space of voltage-dependent capacitance	-30.14			
csd_bw	V	Transition width of voltage-dependent capacitance	47.927			
dgs1	A/mm	Gate leakage prefactor	4.3E-07			
dgs2	A/mm	Gate leakage prefactor	2.6E-13			
dgs3	V	Gate leakage bias dependence parameter	0.8			
dgs4	V	Gate leakage bias dependence parameter	0.23			

Parameters ranges set according to observed variation come from fitting the slow corner device, with 7.6% higher Rds(on). No fast device was measured, parameters are assumed to be symmetrical for slow and fast corners.

4.2. Parameter Extraction

Figure 4.2-1 DC IdVd, Typical, 25 and 150 deg C.



Models will not exactly reproduce the curves shown above, because final models account for additional properties such as the effect of packaging.