Application Guide for the EPC7C019 Evaluation Board

EPC Space (www.epc.space)

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ESD Precaution.

Proper ESD precautions should be employed when handling the EPC7C019 Eval. Board to prevent damage to the components installed on the board.

Introduction.

This document describes functionality, options and the recommended connection of the EPC7C019 EPC7011L7 POL Eval. Board to power supplies, electronic loads and monitoring instruments for proper operation for the evaluation of the switching operation and conversion efficiency performance of the EPC Space EPC7011L7 half-bridge POL power output stage.

This document also provides typical switching performance, typical efficiency performance, the schematic of the evaluation board, the bill of materials (BOM) and the PCB layout of the board in the form of layer-by-layer Gerber rendering of the evaluation printed circuit board.

Please consult the EPC7011L7 data sheet for further details regarding the operation of this integrated circuit.

Evaluation PCB Photograph.

Figure 1a shows the top view and Figure 1b shows the bottom view of the EPC7C019 Eval. Board. These pictures illustrate the component placements, power, load and input signal connections and the numerous test points available for monitoring by the end-user:

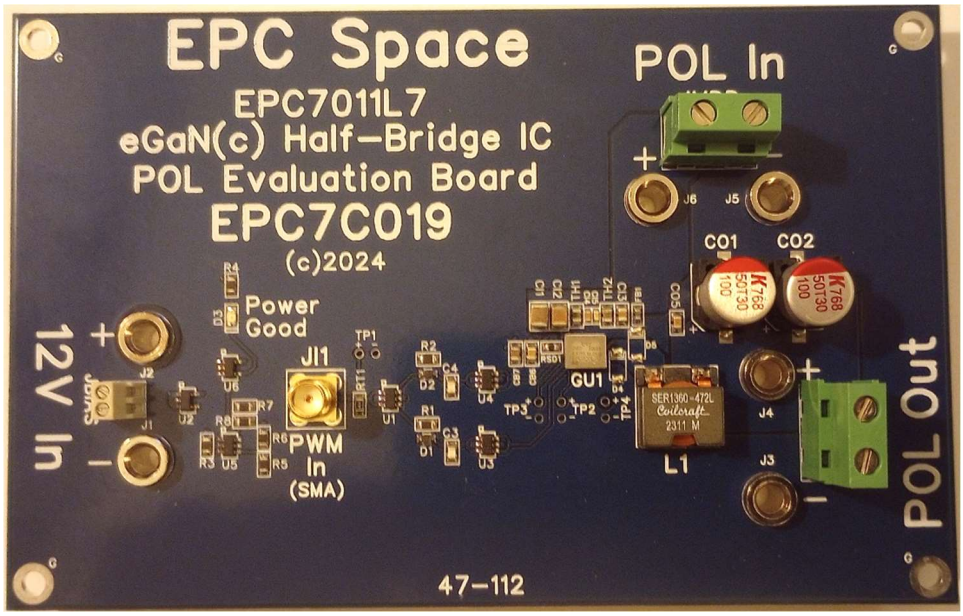

Figure 1a. *EPC7C019 Eval. Board (Top View).*

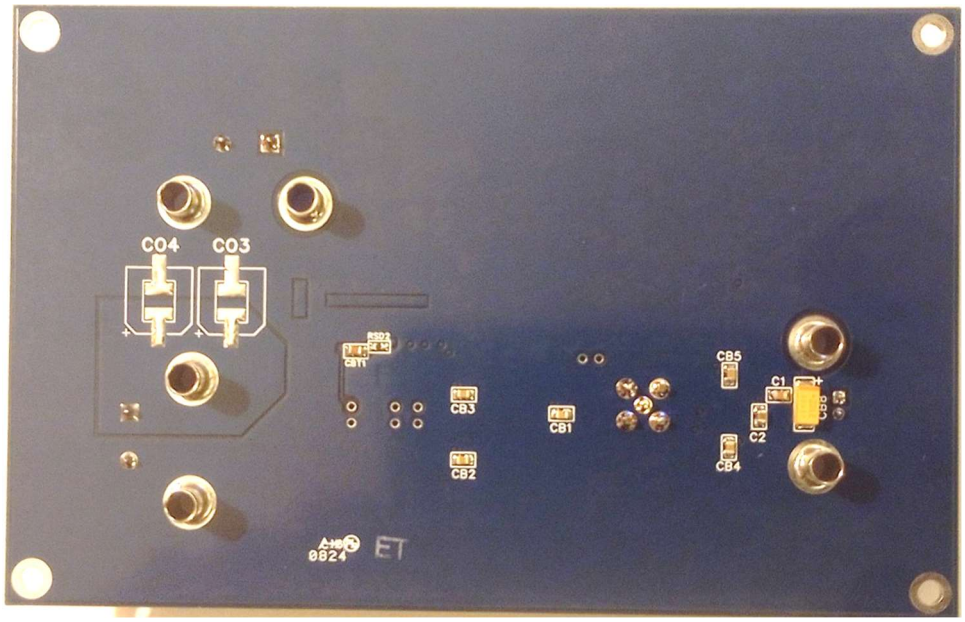

Figure 1b. *EPC7C019 Eval. Board (Bottom View).*

Description of Test Points.

The description of each test point on the EPC7C019 Evaluation Board is found in Table I.

TABLE I. EPC7C019 Evaluation Board Test Point Identification.

Test Point	+/- Spacing (in.)	Parametric Measurement Location
TP1	0.100	PWM Input Signal Monitor.
TP2	0.100	BIN Logic Signal Monitor.
TP3	0.100	TIN Logic Signal Monitor.
TP4	0.100	Switching Node Signal Monitor.

Each set of test points (signal to be measured as indicated by "+", and ground as indicated by "-") have the physical spacings shown in Table I so as to facilitate easy oscilloscope probing by the end-user.

IMPORTANT NOTE: The "-" side of each test point is connected to the ground potential (i.e. 0Vdc) of the Evaluation Board. ALWAYS make sure that the ground connection to the oscilloscope is connected to this point when power is applied to the board as damage may occur to the oscilloscope, the Eval. Board or BOTH.

LOAD AC Signal Monitoring.

Because the EPC7C019 Eval. Board is configured as an "open loop" POL power stage, there is no test point provision for monitoring the AC signal at the output voltage POL Out connections. If it is desired to monitor the ripple voltage at POL Out, then a dual banana jack-to-BNC adapter, Pomona P/N 1269 "BNC (F) To Double Stacking Banana Plug" may be used as the "POL Out" banana jacks are 0.75" similarly-spaced.

Description of Connectors.

There are ten (10) connectors provided on the EPC7C019 Eval. Board. The description of the functionality of each connector is shown in Table II.

TABLE II. EPC7C019 Evaluation Board Connector Description and Functionality.

Connector	Description/Functionality
JI1	0-5V PWM Input Signal/SMA.
JBIAS/J2,J1	+12Vdc bias power supply input.
JOUT/J4,J3	Power output of POL converter.
JVDD/J6,J5	Power input to POL converter.

JI1 "PWM In" Connector Detail.

Connector JI1 is a standard vertical, SMA-style threaded RF connector.

JBIAS Connector Detail.

This connector is a TE 1546215-2 two pin terminal block, screw terminal connector (for VBIAS) as shown in Figure 2:

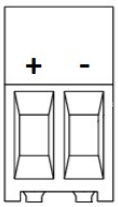

Figure 2. *Connector JBIAS (view facing wire access with polarity shown).*

This connector accepts 16-30AWG wire.

J1 (-) and J2 (+) VBIAS Connector Details.

Connectors J1 and J2 are standard banana jack receptacles.

JOUT Connector Detail.

This connector is a TE 282844-2 two pin terminal block, screw terminal connector (for VOUT) as shown in Figure 3:

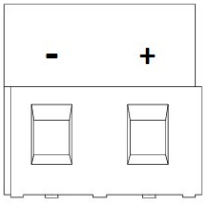

Figure 3. *Connector JVOUT (view facing wire access with polarity shown).*

This connector accepts 12-30AWG wire.

J3 (-) and J4 (+) VOUT Connector Details.

Connectors J3 and J4 are standard banana jack receptacles.

JVDD Connector Detail.

This connector is a TE 282844-2 two pin terminal block, screw terminal connector (for VDD) as shown in Figure 4:

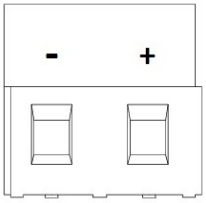

Figure 4. *Connector JVDD (view facing wire access with polarity shown).*

This connector accepts 12-30AWG wire.

J5 (-) and J6 (+) VOUT Connector Details.

Connectors J5 and J6 are standard banana jack receptacles.

"Power Good" LED, D4.

The evaluation board is provided with a visual indication that both VBIAS (12V) and logic (5V) power supplies are in their proper ranges (>11.5V for 12V and >4.5V for 5V) for operation has been provided. Indicator LED D4 glows **GREEN** when VBIAS power is applied and the VDD and VBIAS power supplies are within their proper ranges.

IMPORTANT NOTE: If the "Power Good" LED is not illuminated, then there is either a problem with the VBIAS connection to the PCB, the VBIAS regulator, the on-card drive circuitry or the DUT has been damaged. DO NOT apply or turn-ON VDD to the evaluation board in either case, and contact EPC Space as to how to proceed.

BIN-TIN and TIN-BIN Logic Input Dead Times.

The EPC7C019 Evaluation Board is shipped with a fixed, approximate 20-25ns dead time between the BIN and TIN and TIN and BIN logic inputs being asserted to prevent the possibility of cross-conduction/shoot-through occurring during the evaluation board's operation. The dead time may be modified/increased/decreased by replacing the 15pF (NPO) capacitors in reference designations C3 and C4 with larger/smaller values and by increasing/decreasing the values of resistors R1 and R2.

IMPORTANT NOTE: It is recommended that prior to the application of VDD for testing the evaluation board that the BIN-TIN and TIN-BIN dead times are verified by applying VBIAS to the circuit and monitoring TP2 and TP3 to ensure that the resultant dead times are either 20-25ns (default as shipped) or the desired value if increased/decreased by the end-user

EPC7C019 Recommended Operating Frequency Range and Inductor Ripple Current.

The EPC7C019 Evaluation Board is designed for an operating switching frequency range of 200kHz-2.5MHz. The board, with the components provisioned on it, is designed for a 350-700kHz switching frequency. In operation, the goal in operating the POL power stage is to keep the inductor (L1) ripple current in the range of 0.1 to 0.33 of Iout(max) of the POL power stage. The inductor ripple current is given by:

$$dI_L = ((Vdd *(1 - D)) * (D * Ts)) / L,$$

where Vdd is the power supply voltage to the POL, D is the duty cycle, Ts is the switching period (1/fs) of the PWM input signal and L is the inductor value.

For example, for the full 6A load current capable of being provided by the EPC7011L7 DUT (GU1), the inductor ripple current should be 0.6 to 2Ap-p. So, for the inductor (4.7uH) implemented on the evaluation board, and assuming a VDD of 25Vdc an output voltage of 5V and a switching frequency of 500kHz, the inductor ripple current will be:

$$dI_L = ((25 * (1- (5/25))) * ((5/25) * 2 * 10^{-6})) / 4.7 * 10^{-6} = 1.7Ap\text{-}p$$

This analysis is also valuable for determining the peak inductor current ($I_{LOAD} + dI_L/2$) such that the inductor is **NEVER** allowed to enter saturation. For the inductor incorporated on the evaluation board (Coilcraft SER1360-472KLD), the saturation current is 9.5A (for a 10% inductance decrease). This means that for the operating conditions previously stated, the maximum peak inductor current at maximum load is 6 + 1.7/2 = 6.85A, a value well beneath the saturation current level.

Similar analyses can be performed for the desired operating point/conditions by the end-user to ensure safe operation of the evaluation board. If the inductor current ripple is found to be unsuitable with regards to the design target or with respect to the peak current level, then another inductance value from the Coilcraft SER1360 series (or another vendor's inductor of similar physical dimensions) may be substituted by the end-user.

EPC7C019 Output Capacitors.

The EPC7C019 Evaluation Board is designed with four (4) dual-footprint output capacitor locations: CO1, CO2, CO3 and CO4. Each capacitor location can accept an EIA 1825 ceramic capacitor or a 10mm diameter aluminum or organic polymer electrolytic capacitor (e.g. Kemet A768 Series) such that end-

user may evaluate the performance of a prospective POL output stage with filter components close to the intended design values and types.

As shipped, the EPC7C019 board comes with Kemet A768MS107M1HLAV024 organic polymer capacitors populated in reference designations CO1 and CO2, and with CO3 and CO4 empty (NOPOP).

EPC7011L7 Slowdown Resistors.

The EPC7C019 Evaluation Board is designed to include two (2) "slowdown" resistors for the EPC7011L7 IC. Resistor RSD1, on the top-side of the board just adjacent to the left of GU1, is employed to help slow down, or increase, the rise time of the low-side power switch (from SN-to-PGND). Resistor RSD2, on the bottom-side of the board just beneath GU1, is employed to slow down/increase the rise time of the high-side switch. These two resistors are EIA size 0603, and are deployed as 0R0 value on the as-shipped evaluation board. Because the transition times at the switching node are incredibly fast (under 2ns), the resultant rate-of-change-related voltages and currents can be substantial, particularly the voltages from the parasitic loop inductances in the power switching loop (VDD-PGND). There is only so much effective power loop inductance cancellation and power supply bypassing that can be achieved and deployed. So having RSD1 and RSD2 gives the end-user designer two "knobs" that may be turned to alter the switching node transition times to achieve minimum voltage overshoot at the switching node to prevent voltages beyond the de-rating criteria to be impressed upon GU1. Reducing the transition time slew rates also helps reduce EMI in the circuit, particularly radiated emissions.

The values of RSD1 and RSD2 should be kept in the 0-50 Ohm range. If higher values are desired, it is recommended that the proposed values be subjected to simulation for switching performance in the planned application configuration using the available PSPICE models.

Thermal "Helpers": TH1 and TH2.

The EPC7C019 Evaluation Board is provided with two (2) thermal "helper" locations, populated with aluminum nitride (AlN) thermally-conductive, but electrically isolated, elements TH1 and TH2. These two helpers allow the heat generated by the EPC7011L7 IC (GU1) to be spread over a larger physical area, thus reducing the apparent junction-to-case (Rth(j-c)) thermal resistance of the IC. Components TH1 and TH2 are located within the VDD bypass capacitor field, just above (to the "north") of GU1. These components may be left as deployed in the as-shipped evaluation board, one or the other may be removed to observe the thermal effects or both may be removed – and additional EIA 0805 bypass capacitors may be substituted to help reduce the inevitable leading edge switching spike that is attendant with the quick switching node transition times.

Switching Node "Catch" Diodes: D4 and D5.

The EPC7C019 Evaluation Board is provided with two (2) "catch" diode locations, D4 and D5. These diode PCB shapes are provisioned for an EIA SMA-123FL packaged-diode. Both of these diode locations are not-populated (NOPOP) on the as-shipped evaluation board. Diode D4 should be populated to help reduce dead-time-related power losses, as the Vf of a Schottky diode is less than the Vsd of an eGaN HEMT. Position D5 is provided in case the end-user cannibalizes this evaluation board to use as a half-bridge phase for a motor driver.

EPC7C019 Evaluation Board Minimum and Maximum Ratings.

The EPC7C019 is rated for the following operation:

VDD: 5Vdc to 50Vdc

ILOAD: 0A minimum to 6A maximum.

VBIAS: 12.0Vdc (+/-0.5Vdc),

PWM IN: 0-3.0V minimum/0-5.0V maximum/200kHz to 1.5MHz/95% duty cycle maximum.

Recommended Test Equipment Connections: AC Switching Operation.

Figure 5 shows the recommended connection to/from the Evaluation Board for switching operation.

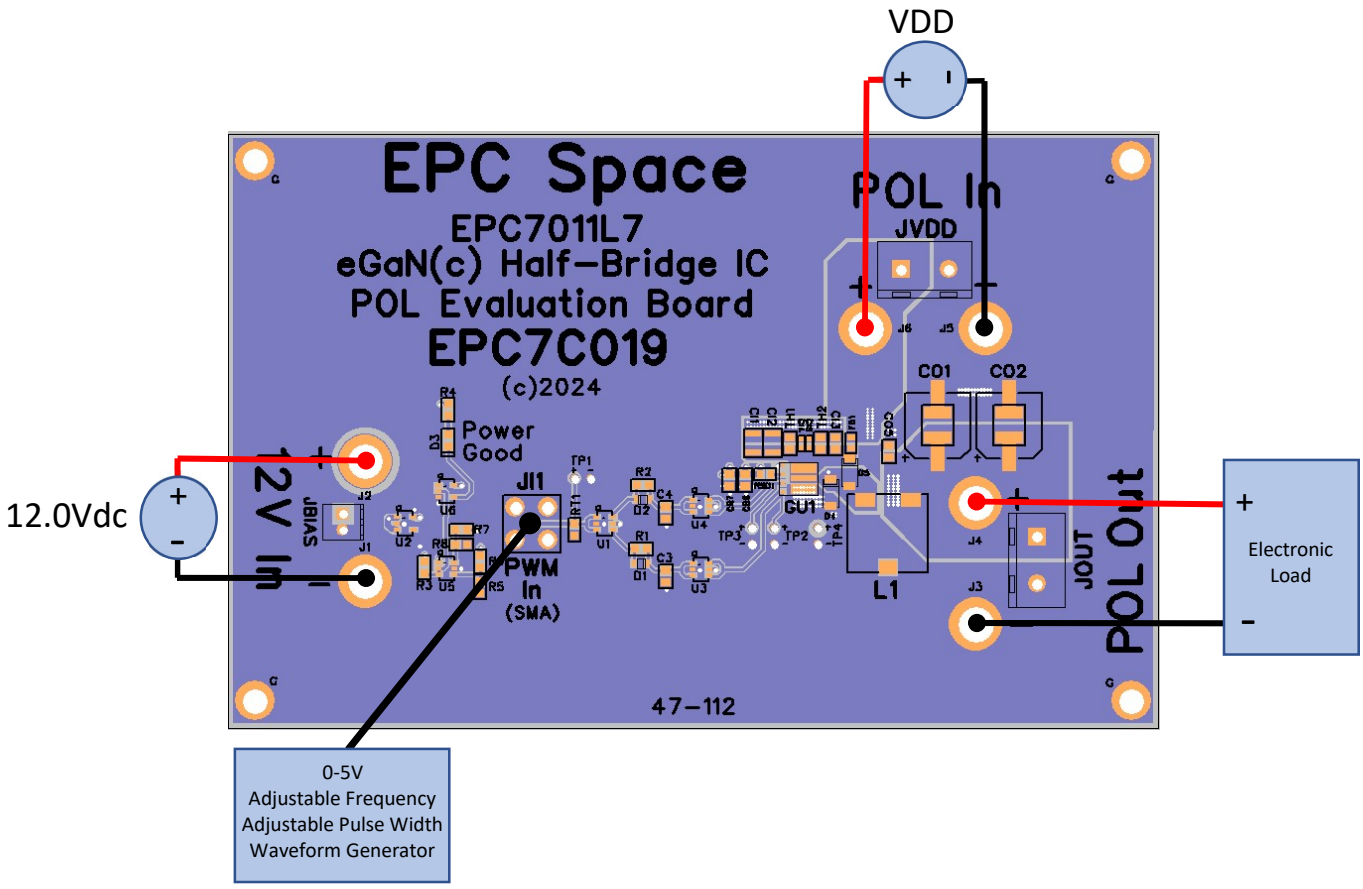

Figure 5. *EPC7C019 Evaluation Board Test Equipment Connections: AC Switching Operation.*

It is recommended that the connections to the EPC7C019 Eval. Board from the VBIAS (12.0V) and VDD power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable.

Recommended Test Equipment: AC Switching Operation.

1.) The following test equipment is recommended to properly evaluate the EPC7C019 Eval. Board as shown in Figure 5:

0-50V, 10A adjustable DC power supply;
0-20V, 100mA adjustable lab power supply set to 12.0Vdc;
50V/10A electronic load;
0-1.5MHz, 0-5V, adjustable duty cycle signal generator;
500MHz two channel oscilloscope;
Two 10:1 passive oscilloscope probes configured with 0.100” spacing between probe tip and ground;
Quantity 6 – 12” to 18” banana plug-to-banana plug cables.

AC Switching Operation Test Procedure.

With the evaluation board connected to the test equipment as shown in Figure 5, the switching node (SN) waveform may be monitored using the following test sequence:

1.) Insert a 0.100" spaced probe/ground into test point TP4, observing the proper polarity for ground;

2.) Apply the desired PWM signal;

3.) Turn on VBIAS;

4.) Adjust the electronic load to the desired output current value and enable the output;

5.) Turn on VDD.

When the POL evaluation circuit is ON and running, the load current (ILOAD) and the PWM duty cycle may be adjusted to obtain the desired value of VLOAD/VOUT.

The resultant SN waveform may be captured for review/analysis.

IMPORTANT NOTE: NEVER adjust the PWM frequency while the EPC7C019 POL circuit is ON and running. Damage/destruction of the FBS GAM02 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks on the evaluation board.

Recommended Test Equipment Connections: Conversion Efficiency.
Figure 6 shows the recommended connection to/from the Evaluation Board for switching operation.

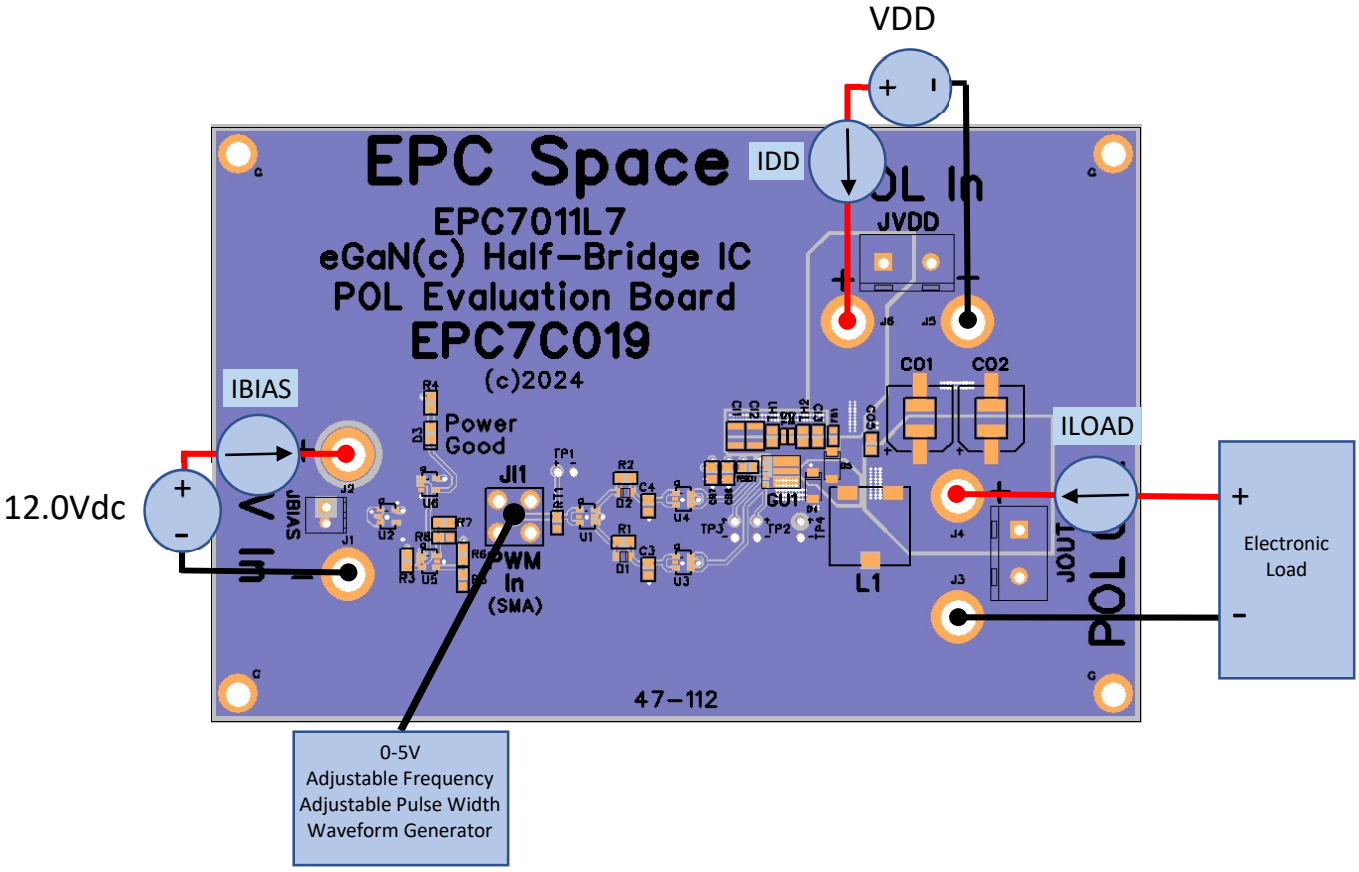

Figure 6. *EPC7011L7 POL Evaluation Board Test Equipment Connections: Conversion Efficiency.*

It is recommended that the connections to the EPC7C019 Eval. Board from the VBIAS (12.0V) and VDD power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable. Voltages VDD, VBIAS and VLOAD should be monitored/measured at the associated banana jacks on the board.

Recommended Test Equipment: Conversion Efficiency.

1.) The following test equipment is recommended to properly evaluate the EPC7C019 Eval. Board as shown in Figure 6:

0-50V, 10A adjustable DC power supply;
0-20V, 100mA adjustable lab power supply set to 12.0Vdc;
50V/10A electronic load;
0-1.5MHz, 0-5V, adjustable duty cycle signal generator;
500MHz two channel oscilloscope;
Two 10:1 passive oscilloscope probes configured with 0.100" spacing between probe tip and ground;
Quantity 3 – Precision digital voltmeters (one to monitor VDD, VBIAS and the load voltage, VLOAD);
Quantity 3 – Precision digital ammeters (one to monitor IDD, IBIAS and the load current, ILOAD);
Quantity 15 – 12" to 18" banana plug-to-banana plug cables.

Conversion Efficiency Test Procedure.

With the evaluation board connected to the test equipment as shown in Figure 6, the conversion efficiency of the POL output stage may be determined at multiple operating points.:

1.) Apply the desired PWM signal, frequency and duty cycle;

3.) Turn on VBIAS;

4.) Adjust the electronic load to the desired output current value and enable the output;

5.) Turn on VDD.

When the POL evaluation circuit is ON and running, the load current (ILOAD) may be increased in small increments and the PWM duty cycle may be adjusted to obtain the desired value of VLOAD/VOUT at each operating point. A most accurate efficiency is obtained if VDD is adjusted to the same value at each value of load current and then the PWM duty cycle is subsequently adjusted to desired value of VLOAD/VOUT.

The conversion efficiency (η) at each operating point is defined as:

$$\eta = (VLOAD * ILOAD) / [(VDD * IDD) + (VBIAS * IBIAS)]$$

IMPORTANT NOTE: **NEVER** adjust the PWM frequency while the EPC7C019 POL circuit is ON and running. Damage/destruction of the EPC7011L7 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks on the evaluation board.

BIN-TIN and TIN-BIN Dead Time Typical Waveforms.

The waveform shown in Figure 7 is typical of the BIN-TIN and TIN BIN dead times for C1 = C2 = 15pF. Logic input BIN is the yellow trace and TIN is blue:

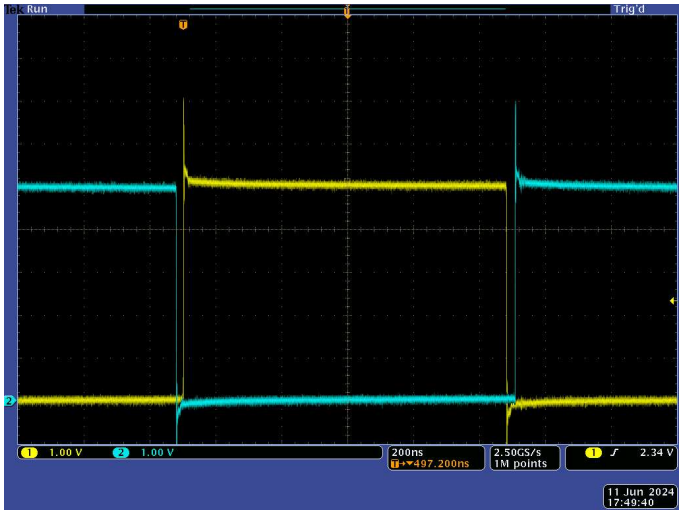

Figure 7. *EPC7C019 Evaluation Board BIN-TIN and TIN BIN Logic Input Dead Time.*

Typical Switching Node (SN) Waveform.

The waveform shown in Figure 8 is typical of the switching node for Eval. Board operation at VDD = 25V, switching frequency = 500kHz, duty cycle = 50% and ILOAD = 6A:

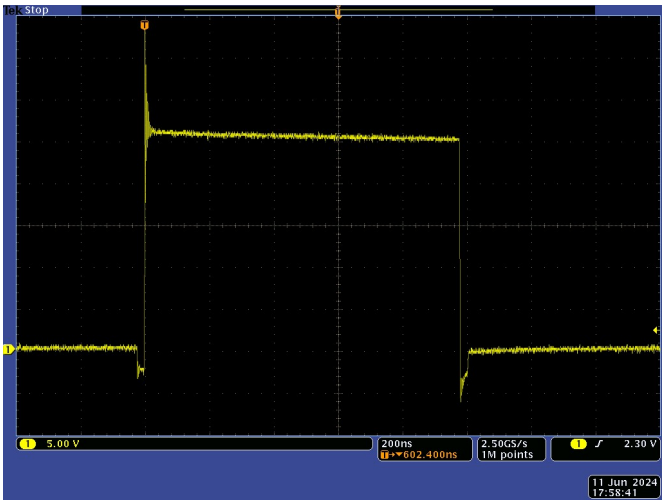

Figure 8. *EPC7011L7 POL Evaluation Board Typical Switching Node Waveform.*

The waveform shown in Figure 9 is typical of the switching node rising transition time for the evaluation board operation under the same conditions as in Figure 8:

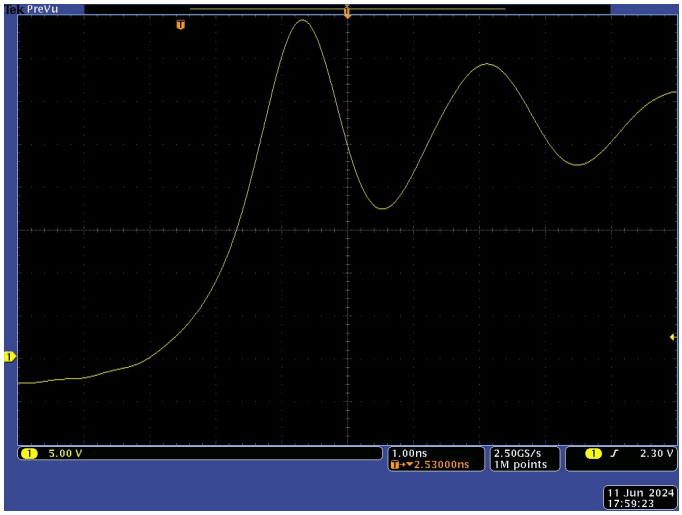

Figure 9. *EPC7011L7 POL Evaluation Board SN Typical Rise Time Waveform.*

The waveform shown in Figure 10 is typical of the switching node falling transition time for the evaluation board operation under the same conditions as in Figure 8:

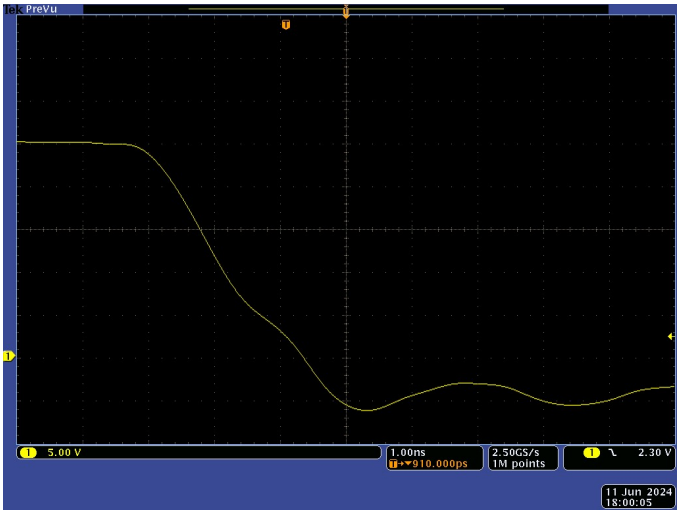

Figure 10. *EPC7011L7 POL Evaluation Board Typical Fall Time Waveform.*

The waveforms shown in Figures 8 and 9 demonstrate the incredibly fast rise/transition times for the switching node of the EPC7011L7 on the EPC7C018 evaluation board, approximately 1-1.2ns. Such a rate-of-change of voltage/current can elicit a large voltage across parasitic inductances in even the best PCB layout and bypass capacitor deployment. Figures 8 and 9 show a nearly 40V peak voltage at the switching node during the ring-out of the parasitic R-L-C circuit formed by real physical components and the parasitic elements in the VDD-to-PGND power loop.

This evaluation board has not been optimized with regards to the switching node leading-edge voltage overshoot level, and the end-user is encouraged to try to reduce the magnitude of this overshoot spike by increasing the values of RSD1 and RSD2, and changing/decreasing the values of VDD bypass capacitors CI1-to CI5, in particular CI3-CI5, to try to gain bypass capacitance effectiveness in the frequency range of the switching node signal's rise time ($0.35 / 1 * 10^{-9}$ = 350MHz). In general, just decreasing the switching node's rising slew rate using RSD2 is enough to reduce the leading-edge voltage spike to a reasonable level. But the ability to adjust the VDD bypass capacitance gives the end-user designer a hip-pocket means to help reduce this rate-of-change-related nuisance even further!

Remember that the dead time MUST be increased because increasing the switching node transition times eats into the dead time, so if either RSD1 or RSD2 is increased in value, the dead times should be increased to a level that safely can accommodate the additional slew-rate-related time increase. Once the desired peak overshoot value is achieved, the dead times may then be reduced until the desired safety margin in switching times is achieved.

As an example, resistor RSD2 was increased to 30 Ohms and the resultant switching node waveform was captured, as shown in Figure 11, for the same conditions defined for Figure 8:

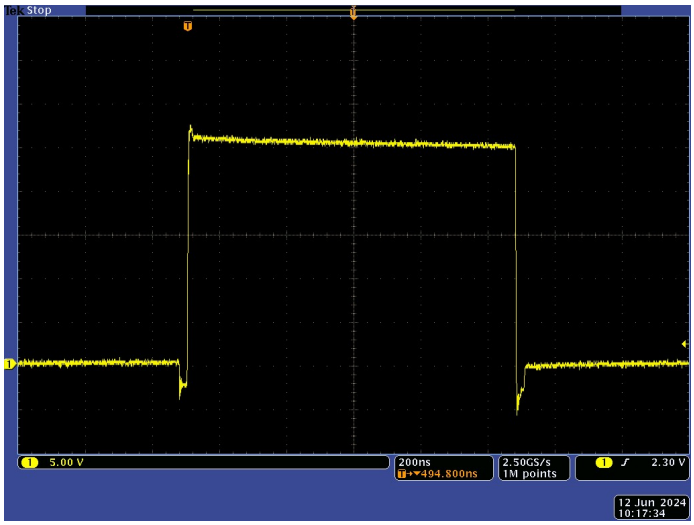

Figure 11. *EPC7011L7 POL Evaluation Board Typical Switching Node Waveform.*

The resultant switching node rising transition time waveform shown in Figure 12 is obtained:

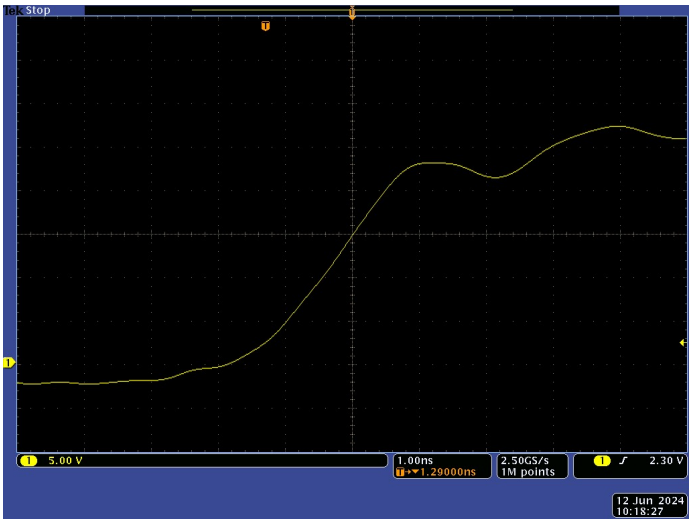

Figure 12. *EPC7011L7 POL Evaluation Board Typical Switching Node Rise Time Waveform.*

It is obvious reviewing Figures 11 and 12 that the 30 Ohm value for RSD2 had greatly reduced the amplitude of the peak value of the leading-edge voltage spike from ~40V (14V spike amplitude) to ~27V (2V spike amplitude). This is due to the switching node rise time being increased to ~2ns.

Understand that in some cases if the dead time is set to be as small as possible that this increase in the switching node's rising transition time will require a commensurate lengthening of the dead times, particularly that of logic input TIN rising to BIN falling -- to ensure that dynamic cross-conduction is avoided. Also understand that a slight efficiency penalty is incurred due to the increase in the switching loss for the switching node rise time. For the conditions described for Figure 8, these losses were originally 37.5mW for the 0 (zero) Ohm value of RSD2. With RSD2 set to 30 Ohms, this loss doubles to 75mW. Not a considerable increase in this situation, but nonetheless an increase noteworthy of mention.

Typical Conversion Efficiency Graphs.

The graph shown in Figure 13 is typical of the EPC7C019 evaluation board conversion efficiency with respect to various switching frequencies, for the conditions listed on the graph:

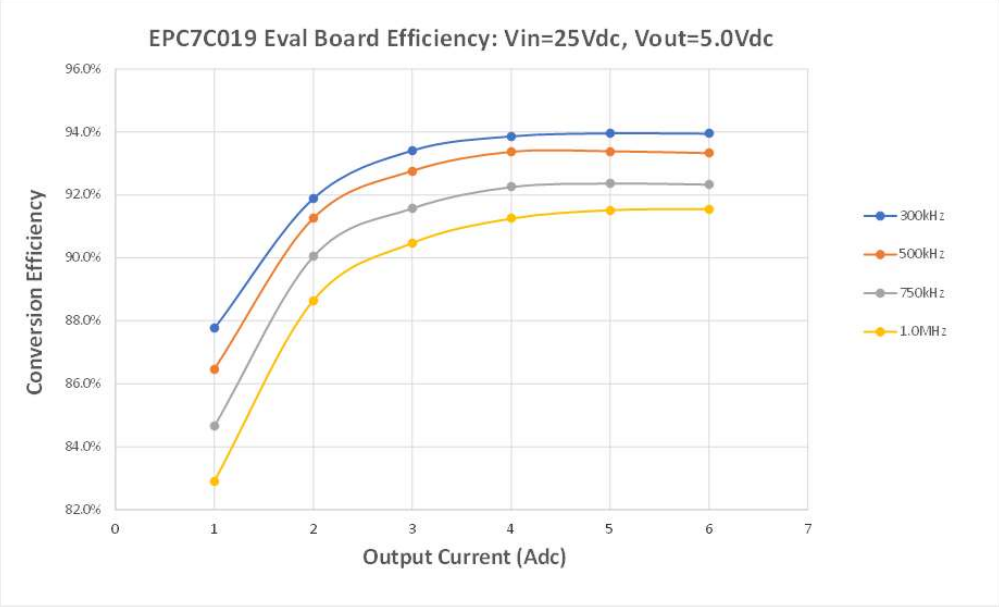

Figure 13. *EPC7011L7 POL Evaluation Board Typical Conversion Efficiency vs Frequency.*

The graph shown in Figure 14 is typical of the EPC7C019 evaluation board conversion efficiency at a switching frequency of 500kHz for various duty cycles, for the conditions listed on the graph:

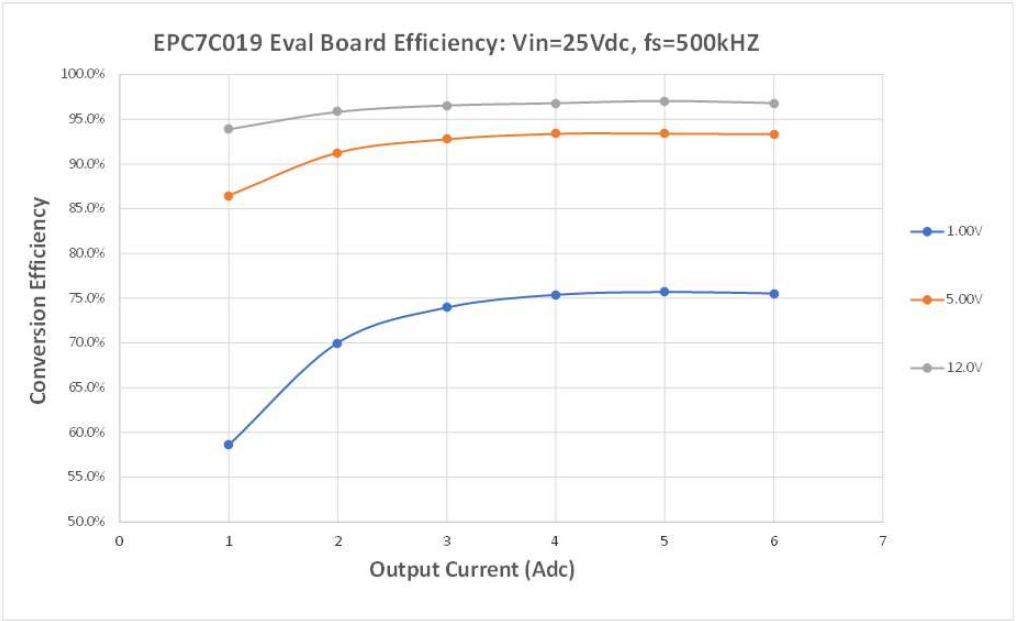

Figure 14. *EPC7011L7 POL Evaluation Board Typical Conversion Efficiency: 500kHz.*

Optimization of Conversion Efficiency Performance.

No attempt has been made to optimize the conversion efficiency performance of the EPC7C019 EPC7011L7 POL evaluation board. The board was, however, optimized for switching performance and to provide the best switching waveforms in terms of minimizing stray inductances in the power loop to prevent transient overshoots at the switching node and VDD. Even so, due to the nature of the EPC7011L7 IC (GU1) as part power and part RF device due to its impressive switching characteristics, the board exhibits a high voltage overshoot value during the switching node's rising transition time.

Because the evaluation board was intended to be used over a wide range of input and output voltages, load currents and switching frequencies, there could be no "optimized" set of components used for all possible applications to achieve the highest possible conversion efficiency. As such, optimization of the evaluation board for a particular customer end-use application is left to the designer who is evaluating this board. To this end, the output inductor L1 may be changed for a different value in the same package style. The inductor utilized on the evaluation board is in the Coilcraft SER1360, so other inductance values (with lower DC resistances and AC core losses) may be chosen for the particular switching frequency desired.

The end-user is invited to change component values or cut-in their planned components for their design using the EPC7C019 board as their starting point. It provided a convenient vehicle for achieving the desired performance results in a very short amount of time!

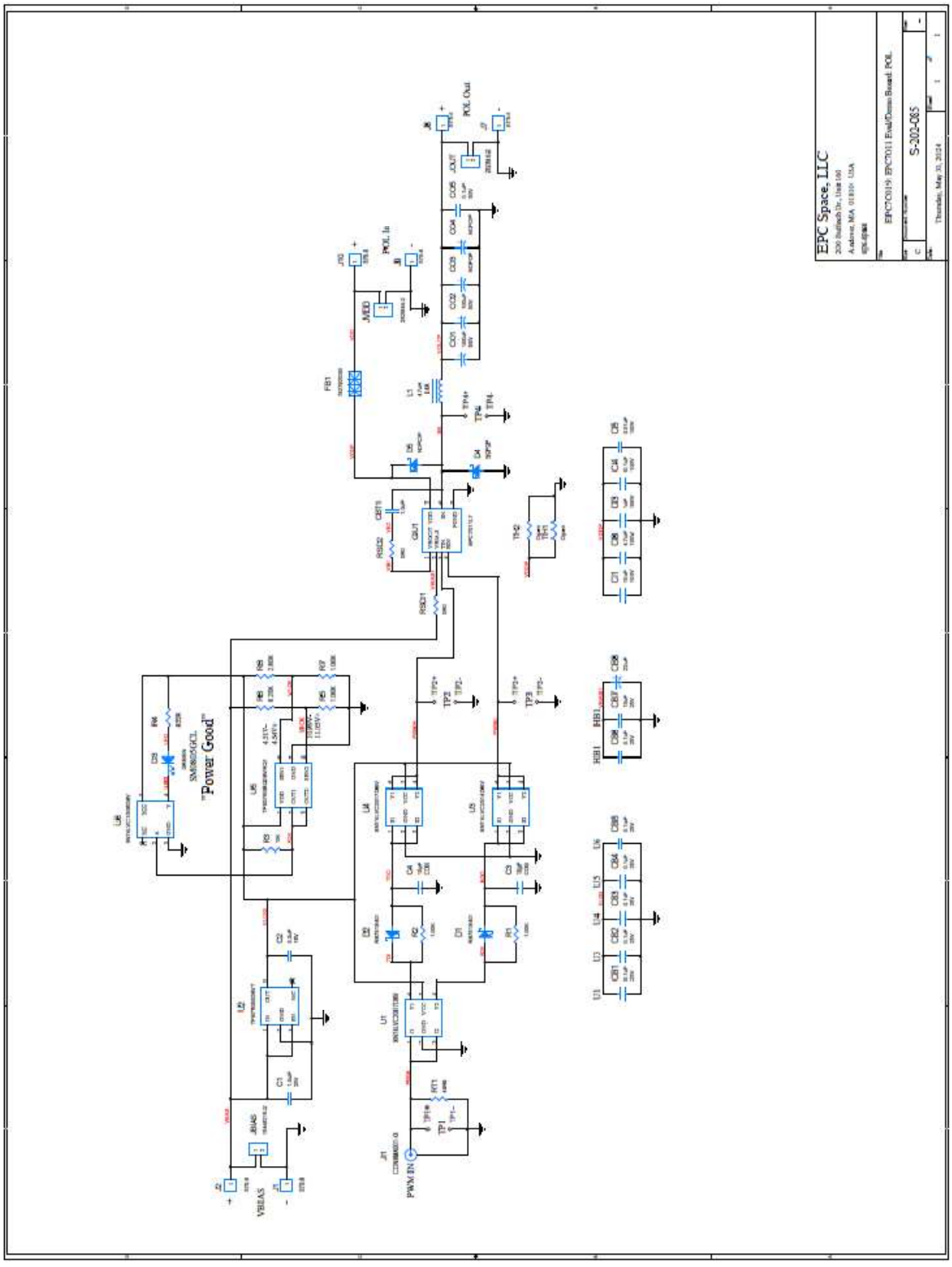

Figure 15. *EPC7C019/EPC7011L7 POL Evaluation Board Schematic Diagram.*

[**NOTE:** The above schematic is recognized and understood to be an eye-test for the reader due to its low resolution, and a higher-resolution PDF version may be obtained upon request from EPC Space.]

EPC7C019 / EPC7011L7 POL Evaluation Board BOM

The BOM for the EPC7C019 POL Evaluation Board is shown in Table III.

Table IV. EPC7C019/EPC7011L7 POL Evaluation Board Bill of Materials.

Item	Quantity	Ref. Des.	Description/Value	Mfgr.	Mfgr. P/N	Size/Package	Notes/Comments
1	6	J1,J2,J3,J4,J5,J6	Staking Banana Jack, Uninsulated	Keystone	575-8	0.208" Dia. Hole	Install at each 0.208" diameter hole.
2	2	C1,CBT1	1.0uF/50V/X7R/10%/0805/Ceramic Capacitor	AVX/Kyocera	08055C105K4T4A	C0805	1uF/50V
3	1	C2	3.3uF/25V/X7R/10%/0805/Ceramic Capacitor	TDK	C2012X7R1E335K125AB	C0805	3.3uF/25V
4	2	C3,C4	15pF/50V/COG/2%/0805/Ceramic Capacitor	Kemet	C0805C150F5GACAUTO	C0805	15pF/50V
5	7	CB1,CB2,CB3,CB4,CB5,CB6,CO5	0.1uF/50V/X7R/10%/0805/Ceramic Capacitor	Kemet	C0805C104K5RECAUTO	C0805	0.1uF/50V
6	1	CB7	10uF/25V/X7R/10%/0805/Ceramic Capacitor	Murata	GRM21BZ71E106KE15L	C0805	10uF/25V
7	1	CB8	22uF/25V/Tantalum/10%/C Case/Tantalum SMT Capacitor	Kemet	T95C226K025RSG400	TANT_C	22uF/25V. Observe polarity when placing.
8	1	C11	10uF/100V/X7R/10%/1210/Ceramic Capacitor	TDK	C3225X7R2A106K250AC	C1210	10uF/100V
9	1	C12	4.7uF/100V/X7R/10%/1210/Ceramic Capacitor	AVX/Kyocera	KAM32LR72A475KU	C1210	4.7uF/100V
10	1	C13	1.0uF/100V/X7R/10%/0805/Ceramic Capacitor	AVX/Kyocera	08051C105K4T2A	C0805	1uF/100V
11	1	C14	0.1uF/100V/X7R/10%/0603/Ceramic Capacitor	AVX/Kyocera	KAM15BR72A104KT	C0603	0.1uF/100V
12	1	C15	0.01uF/100V/X7R/10%/0603/Ceramic Capacitor	AVX/Kyocera	06031C103K4T2A	C0603	0.01uF/100V
13	2	CO1,CO2	100uF/50V/Alum. Org. Polymer/20%/10mm x16.5mm SMT Capac	Kemet	A768MS107M1HLAV024	A768MS107M1HLAV024	100uF/50V. Observe polarity when placing.
14	2	D1,D2	0.12A/40V/SOD-323/Schottky Diode	ON Semi	RB751V40T1G	SOD-323	Observe polarity/orientation when placing.
15	1	D3	568nm Green Water Clear/0805 Package LED	Bivar	SM0805GCL	D0805	Observe polarity/orientation when placing.
16	NOPOP	D4,D5	2A/100V/SOD-123Flat/Schottky Diode	ST	STPS1H100ZF	SOD123Flat	NOPOP
17	1	FB1	5A/8.5 Ohm/0.004 Ohms/Ferrite Bead	Murata	BLE18PS080BH1D	R0603	
18	1	GU1	EPC7011/Half-Bridge IC/LL7 Package	EPC Space	EPC7011L7	EPCS L7	
19	1	J11	SMA/Vertical/50 Ohms/Brass-Gold/SMT	Linx Tech.	CONSMA001-G	CONSMA001-G	
20	1	JBIAS	2 Position/2.54mm/150V/Fixed Terminal Block	TE	1546215-2	1546215-2	
21	1	JVDD,JOUT	2 Position/7.5mm/300V/Fixed Terminal Block	TE	282844-2	282844-2	
22	1	L1	9.4A/4.7uH Power Inductor/6.05 milliohms/13mm x 13mm	Bourns	SER1360-472KLD	SER1360	
23	1	R4	422R/1%/0805/Thick Film Chip Resistor	Vishay	CRCW0805422RFKEA	R0805	422R
24	2	RSD1,RSD2	0R0/1%/0603 Thick Film Jumper Chip Resistor	Vishay	RCC06030000Z0EA	R0603	0R0
25	4	R1,R2,R3,R7	1.0K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08051K00FKEA	R0805	1.0K
26	1	R3	10.0K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW080310K0FKEA	R0805	10.0K
27	1	R6	8.25K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08058K25FKEA	R0805	8.25K
28	1	R8	2.80K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08052K80FKEA	R0805	2.80K
29	1	RT1	49R9/1%/0805 Thick Film Chip Resistor	Panasonic	ERJ-P06F49R9V	R0805	
30	2	TH1,TH2	AlN Thermal "Helper" Chip/0.025" th/Wraparound Term/0805	IMS	BGR-0805WA	R0805	
31	1	U1,U4	nal Schmitt-Trigger Buffer/Little Logic/1.65-5.5V/LVC/SOT-23-	TI	SN74LVC2G17DBVR	SOT-23-6	Observe polarity/orientation when placing
32	1	U2	5V/50mA LDO Regulator/6.3V/SOT-23-5	TI	TPS76550DBVT	SOT-23-5	
33	1	U3	al Schmitt-Trigger Inverter/Little Logic/1.65-5.5V/LVC/SOT-2	TI	SN74LVC2G14DBVR	SOT-23-6	Observe polarity/orientation when placing
34	1	U5	Dual Voltage Supervisor/Open Drain/5V/1%/SOT-23-6	TI	TPS3780BQDBVRQ1	SOT-23-6	Observe polarity/orientation when placing
35	1	U6	ngle Open-Drain Inverter/Little Logic/1.65-5.5V/LVC/SOT-23-	TI	SN74LVC1G06DBVR	SOT-23-5	
36	6	Hardware	Spacer/Hex/Aluminum/6-32/2-1/8" Length	Essentra	14HTSP008	N/A	
37	6	Hardware	Screw/6-32/Nylon/Round head/Slotted/0.5" Length	Essentra	010632R050	N/A	
38	1	PCB	5.82" x 3.72" x 0.063", 6 Layer FR-4 PCB, Double-Sided	4PCB.com	47-101-A	N/A	

Printed Circuit Board and Layout Details.

The printed circuit board (PCB) for the EPC7C019 EPC7011L7 POL Evaluation Board is constructed with four layers. The PCB is 5.82" x 3.72" and is 0.063" thick. The outer layers are 2 oz/in^2 and the inner layers are 1 oz/in^2 copper etch. All electronic components are SMT-packages and all connectors are through-hole.

The individual Gerber layers for the PCB are shown in Figures 16 to 24, following:

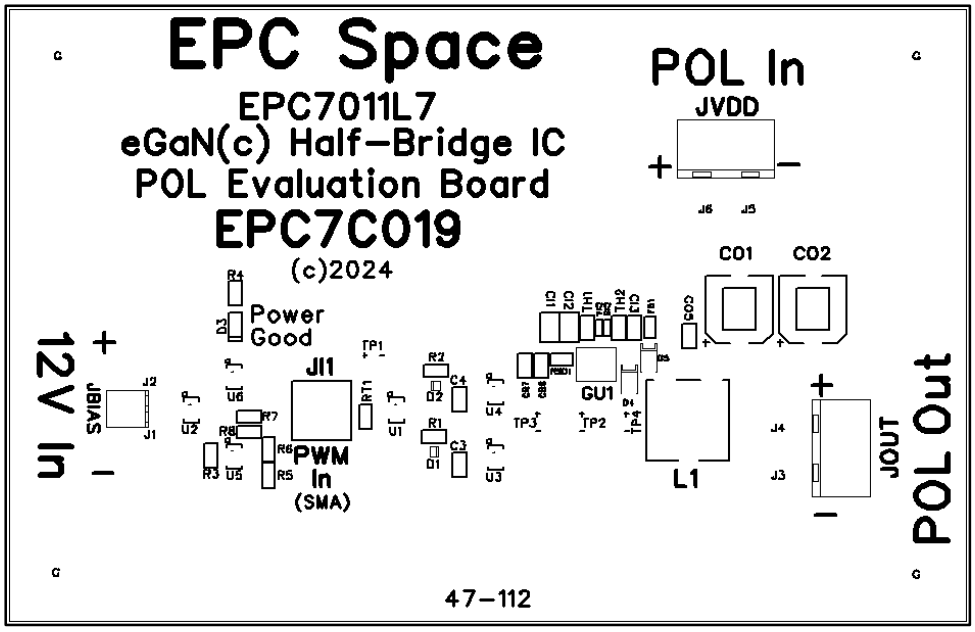

Figure 16. *EPC7C019/EPC7011L7 POL Evaluation Board Top Silkscreen.*

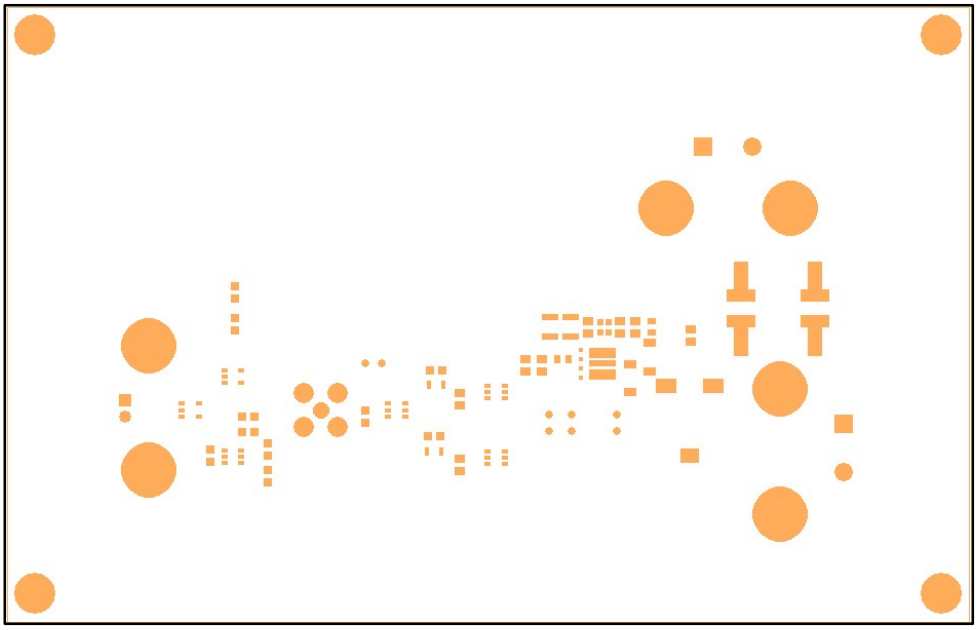

Figure 17. *EPC7C019/EPC7011L7 POL Evaluation Board Top Solder Mask.*

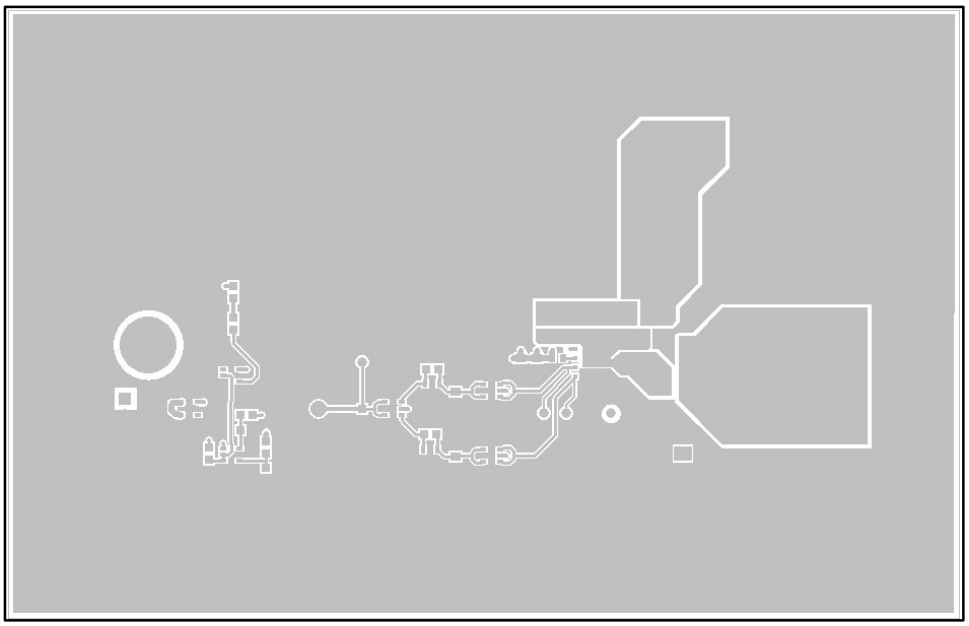

Figure 18. *EPC7C019/EPC7011L7 POL Evaluation Board Top Copper Etch (2 oz).*

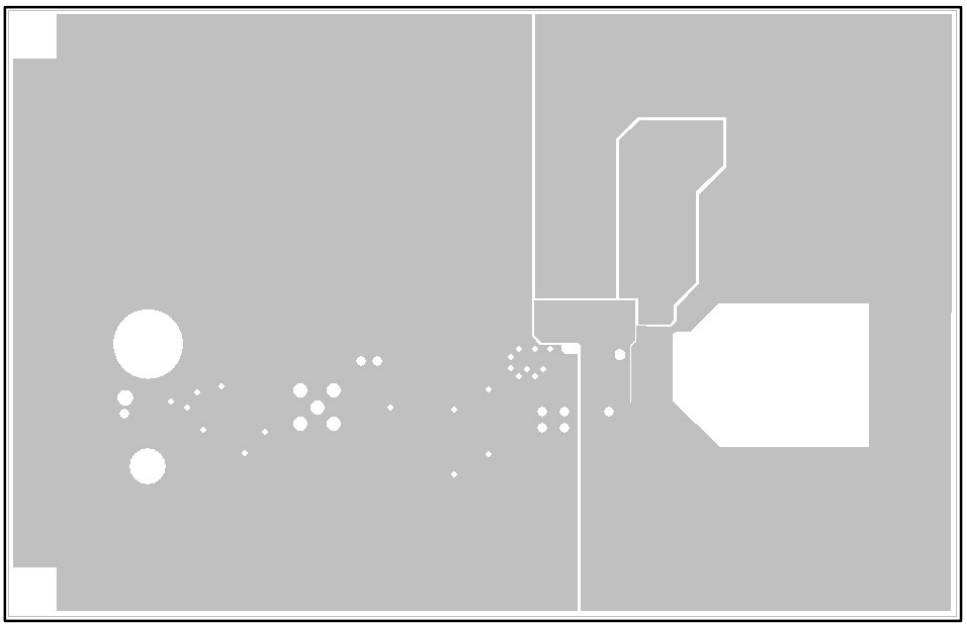

Figure 19. *EPC7C019/EPC7011L7 POL Evaluation Board Inner Layer 1 Copper Etch (1 oz).*

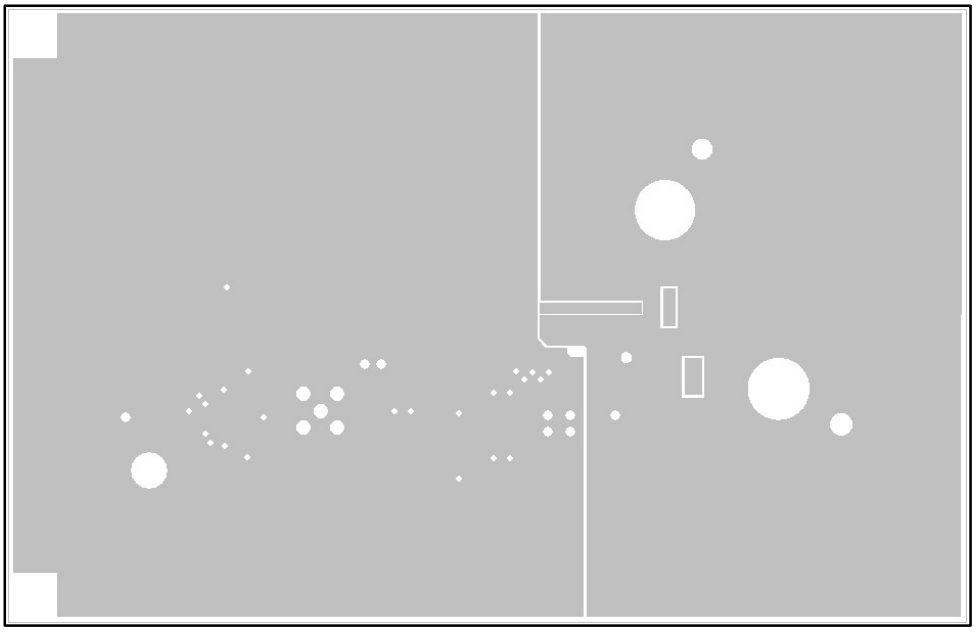

Figure 20. *EPC7C019/EPC7011L7 POL Evaluation Board Inner Layer 2 Copper Etch (1 oz).*

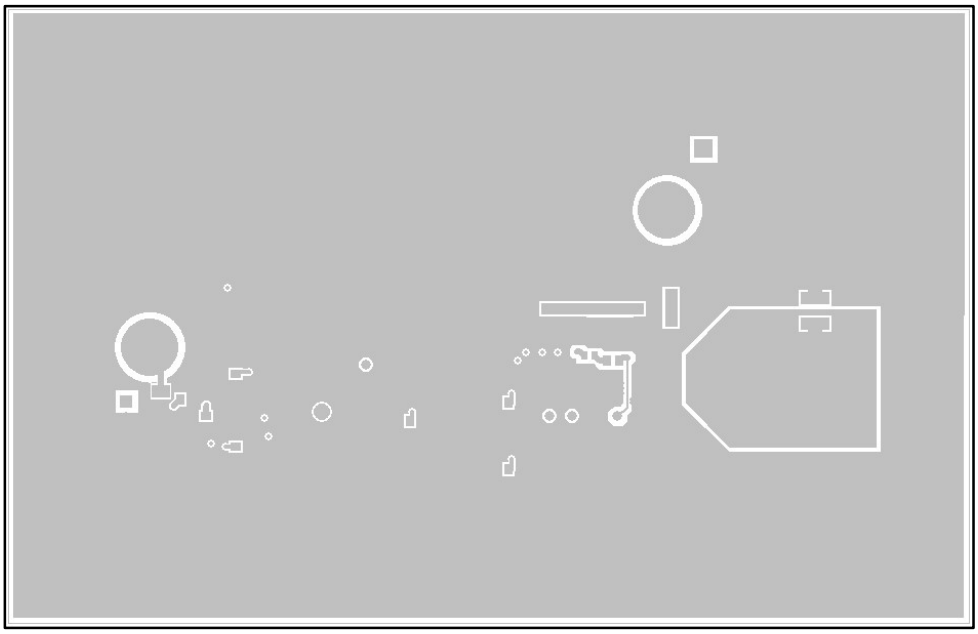

Figure 21. *EPC7C019/EPC7011L7 POL Evaluation Board Bottom Copper Etch (2 oz).*

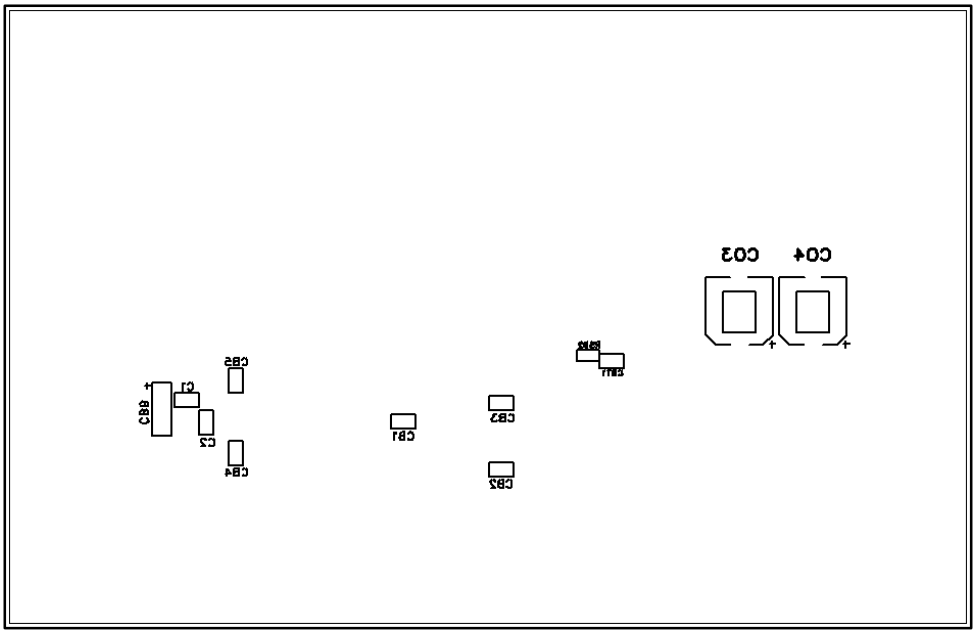

Figure 22. *EPC7C019/EPC7011L7 POL Evaluation Board Bottom Silkscreen.*

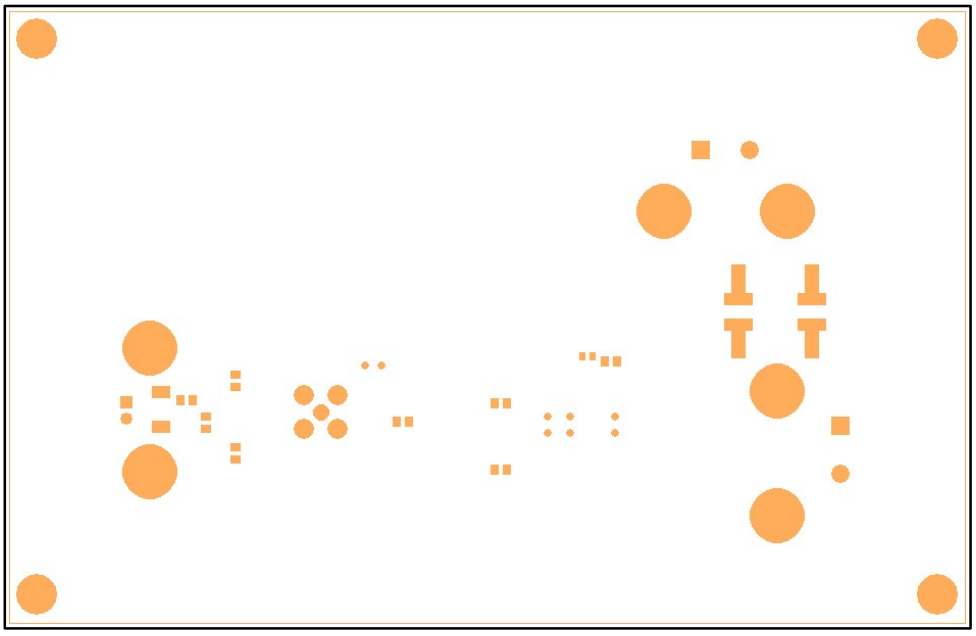

Figure 23. *EPC7C019/EPC7011L7 POL Evaluation Board Bottom Solder Mask.*

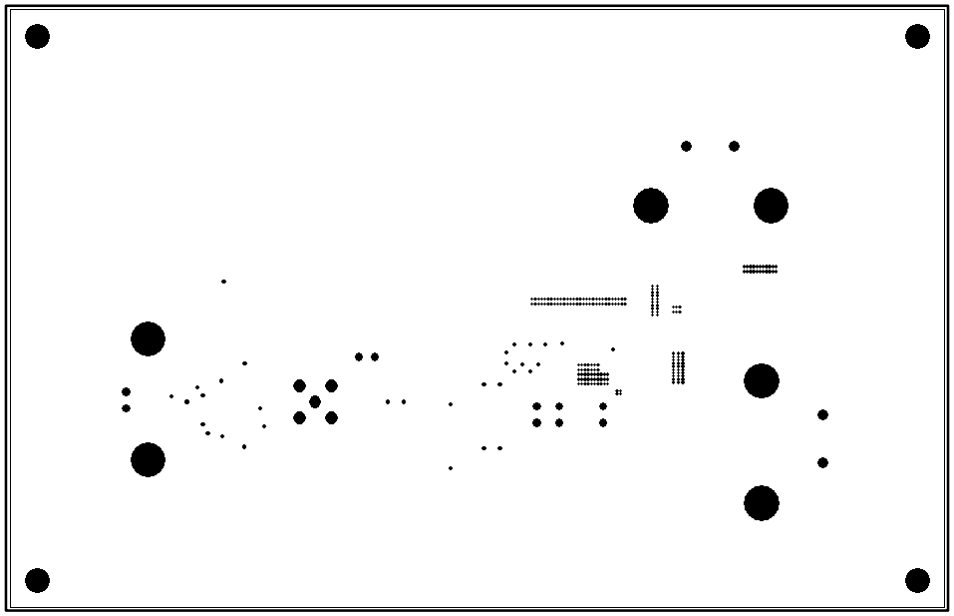

Figure 24. *EPC7C019/EPC7011L7 POL Evaluation Board Drill Pattern.*

NOTES:

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Revisions:

Revision	Date	Status
PR	6/12/2024	Pre-Release
--		Release
A		Revision A

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