Application Guide for the EPC7C020 Evaluation Board

ESD Precaution

Proper ESD precautions should be employed when handling the EPC7C020 Eval. Board to prevent damage to the components installed on the board.

Introduction

This document describes functionality, options and the recommended connection of the EPC7C020 EPC7011L7 Boost Eval. Board to power supplies, electronic loads and monitoring instruments for proper operation for the evaluation of the switching operation and conversion efficiency performance of the EPC Space EPC7011L7 half-bridge Boost power output stage.

This document also provides typical switching performance, typical efficiency performance, the schematic of the evaluation board, the bill of materials (BOM) and the PCB layout of the board in the form of layer-by-layer Gerber rendering of the evaluation printed circuit board.

Please consult the EPC7011L7 data sheet for further details regarding the operation of this integrated circuit.

Evaluation PCB Photograph

Figure 1 shows the top view of the EPC7C020 Eval. Board. This picture illustrates the component placements, power, load and input signal connections and the numerous test points available for monitoring by the end-user:

Figure 1. *EPC7C020 Eval. Board (Top View).*

Description of Test Points

The description of each test point on the EPC7C020 Evaluation Board is found in Table I.

TABLE I. EPC7C020 Evaluation Board Test Point Identification.

Test Point	+/- Spacing (in.)	Parametric Measurement Location
TP1	0.100	PWM Input Signal Monitor.
TP2	0.100	BIN Logic Signal Monitor.
TP3	0.100	TIN Logic Signal Monitor.
TP4	0.100	Switching Node Signal Monitor.

Each set of test points (signal to be measured as indicated by "+", and ground as indicated by "-") have the physical spacings shown in Table I so as to facilitate easy oscilloscope probing by the end-user.

> **NOTE:** The "-" side of each test point is connected to the ground potential (i.e. 0Vdc) of the Evaluation Board. ALWAYS make sure that the ground connection to the oscilloscope is connected to this point when power is applied to the board as damage may occur to the oscilloscope, the Eval. Board or BOTH.

LOAD AC Signal Monitoring

Because the EPC7C020 Eval. Board is configured as an "open loop" Boost power stage, there is no test point provision for monitoring the AC signal at the output voltage Boost Out connections. If it is desired to monitor the ripple voltage at Boost Out, then a dual banana jack-to-BNC adapter, Pomona P/N 1269 "BNC (F) To Double Stacking Banana Plug" may be used as the "Boost Out" banana jacks are 0.75" similarly-spaced.

Description of Connectors

There are ten (10) connectors provided on the EPC7C020 Eval. Board. The description of the functionality of each connector is shown in Table II.

TABLE II. EPC7C020 Evaluation Board Connector Description and Functionality.

Connector	Description/Functionality
JI1	0-5V PWM Input Signal/SMA.
JBIAS/J2,J1	+12Vdc bias power supply input.
JOUT/J4,J3	Power output of Boost converter (Vout).
JVDD/J6,J5	Power input to Boost converter (VDD).

JI1 "PWM In" Connector Detail

Connector JI1 is a standard vertical, SMA-style threaded RF connector.

JBIAS Connector Detail

This connector is a TE 1546215-2 two pin terminal block, screw terminal connector (for VBIAS) as shown in Figure 2:

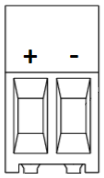

Figure 2. *Connector JBIAS (view facing wire access with polarity shown).*

This connector accepts 16-30AWG wire.

J1 (-) and J2 (+) VBIAS Connector Details

Connectors J1 and J2 are standard banana jack receptacles.

JOUT Connector Detail

This connector is a TE 282844-2 two pin terminal block, screw terminal connector (for VOUT) as shown in Figure 3:

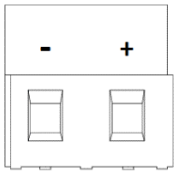

Figure 3. *Connector JOUT (view facing wire access with polarity shown).*

This connector accepts 12-30AWG wire.

J5 (-) and J6 (+) VOUT Connector Details

Connectors J5 and J6 are standard banana jack receptacles.

JVDD Connector Detail

This connector is a TE 282844-2 two pin terminal block, screw terminal connector (for VDD) as shown in Figure 4:

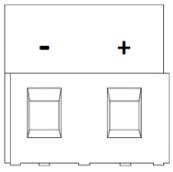

Figure 4. *Connector JVDD (view facing wire access with polarity shown).*

This connector accepts 12-30AWG wire.

J3 (-) and J4 (+) VDD Connector Details

Connectors J3 and J4 are standard banana jack receptacles.

"Power Good" LED, D3

The evaluation board is provided with a visual indication that both VBIAS (12V) and logic (5V) power supplies are in their proper ranges (>11.5V for 12V and >4.5V for 5V) for operation has been provided. Indicator LED D3 glows **GREEN** when VBIAS power is applied and the VDD and VBIAS power supplies are within their proper ranges.

NOTE: If the "Power Good" LED is not illuminated, then there is either a problem with the VBIAS connection to the PCB, the VBIAS regulator, the on-card drive circuitry or the DUT has been damaged. DO NOT apply or turn on VDD to the evaluation board in either case, and contact EPC Space as to how to proceed.

BIN-TIN and TIN-BIN Logic Input Dead Times

The EPC7C020 Evaluation Board is shipped with a fixed, approximate 20-25ns dead time between the BIN and TIN and TIN and BIN logic inputs being asserted to prevent the possibility of cross-conduction/shoot-through occurring during the evaluation board's operation. The dead time may be modified/increased/decreased by replacing the 15pF (NPO) capacitors in reference designations C3 and C4 with larger/smaller values and by increasing/decreasing the values of resistors R1 and R2.

NOTE: It is recommended that prior to the application of VDD for testing the evaluation board that the BIN-TIN and TIN-BIN dead times are verified by applying VBIAS to the circuit and monitoring TP2 and TP3 to ensure that the resultant dead times are either 20-25ns (default as shipped) or the desired value if increased/decreased by the end-user.

Duty Cycle Limitations and Input Fuse

Like any boost converter, the EPC7C020 board has limitations on the useful range that the duty cycle applied to it may assume, either to guarantee the output is boosted (increased in magnitude) from the input or to prevent damage/destruction of the EPC7011L7 IC. Figure 5 shows the boost factor, V_{out}/V_{in}, for duty cycles from 0% to 95% (0.95), and at two different conversion efficiencies 90% (blue) and 100% (green, ideal). The boost factor for the EPC7C010 will vary between the two values shown for a given duty cycle, depending upon the components utilized. For the EPC7C020 board as supplied, the boost factor will be closer to the ideal than to the 90% efficiency value. The 95% duty cycle value should be considered the upper limit for the EPC7C020 during operation.

The boost factor for the EPC7C020, accounting for the circuit's efficiency is:

$$\mathbf{Vout/Vin = \eta / (1 - D),}$$

Where η is the estimated efficiency and D is the duty cycle.

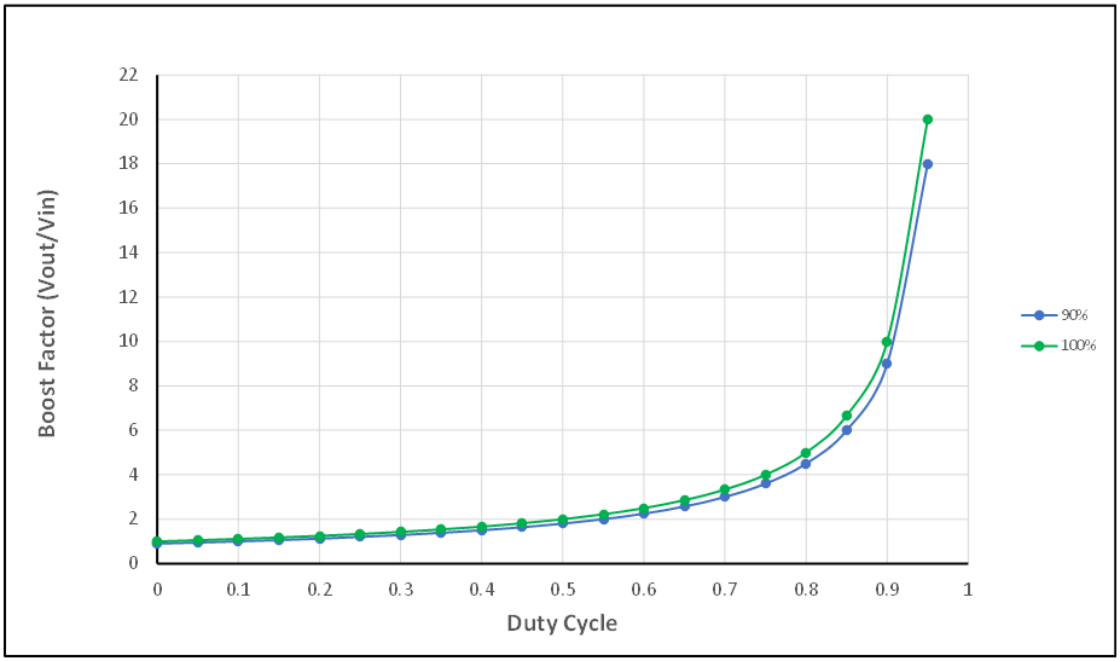

Figure 5. *EPC7C020 Evaluation Board Boost Factor vs. Duty Cycle.*

The curves show that the boost factor will be two (2) or less for duty cycles 50% or less. Obviously for a duty cycle of zero (0), the duty cycle will be V_{in}. But actually, unless the external boost diode D5 is included in the circuit, the output will decay to a value less than Vin, as the bootstrap capacitor for the high-side switch in the EPC7011L& IC will discharge. This situation will render that switch (the synchronous boost diode function) inoperative, and the high-side switch of the EPC7011L7 IC will enter 3rd quadrant bias regime.

For a duty cycle of 100%, the main power switch to ground is continuously closed, providing VDD across the inductor in a continuous manner. After the brief period of time it takes for the inductor L1 to saturate, the current drawn from the VDD power source through the inductor and main power switch will be limited only by the DC resistance of the inductor and the power switch. This current will be uncontrolled and enormous, and will cause the power switch in the EPC7011L7 to overheat and be destroyed.

To prevent this situation, in case of an accidental application of a 100% duty cycle, a fuse is incorporated in-line with the input power supply to the boost converter. This fuse, F1, is an 8A, 125V, fast blow type (Schurter P/N 3404.0020.22). The end-user may replace this fuse with a SMALLER value fuse of the similar physical size to suit the particular requirements of their application.

EPC7C020 Maximum Output Current vs Duty Cycle

The EPC7C020 Evaluation Board is rated for a minimum input voltage of 5V and maximum output voltage of 40Vdc. The EPC7011L7 IC is rated for 6A, maximum. These three input-output voltage and current restrictions place similar restrictions on the available maximum output current for a given duty cycle and input voltage. Since the output power must equal the input power, with the conversion efficiency considered, the maximum output current for a given input and output voltage is:

$$\mathbf{Iout = (Vin * Iout(max)) / (Vout * \eta),}$$

where Iout(max) = 6A and η = 0.95 (95%).

Figure 6 shows the maximum output current for the EPC7C020 board for Vout = 15V (green) and Vout = 30V (blue) for input voltages of 5 to 40V. It can be seen that the 15V output case reaches the 6A maximum current rating for input voltages just above 15V, while the output current never reaches the 6A level at the maximum input voltage for the 30V output.

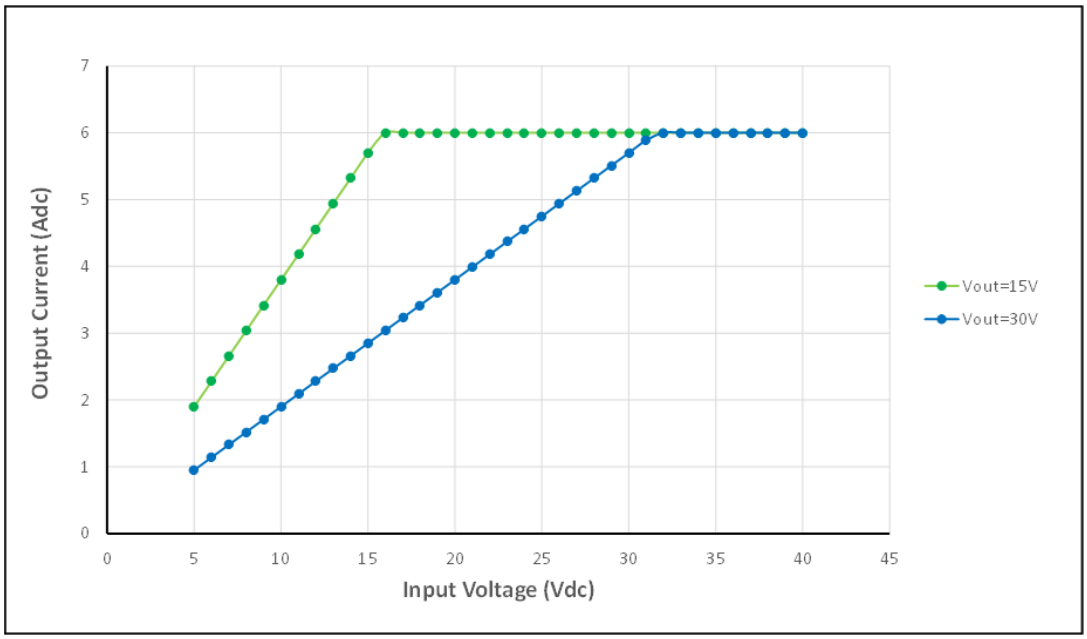

Figure 6. *EPC7C020 Evaluation Board Maximum Output Current versus Input Voltage and Output Voltage.*

EPC7C020 Recommended Operating Frequency Range and Inductor Ripple Current

The EPC7C020 Evaluation Board is designed for an operating switching frequency range of 200kHz-1.5MHz. The board, with the components provisioned on it, is designed for a 200-500kHz switching frequency. In operation, the goal in operating the boost power stage is to keep the inductor (L1) ripple current in the range of 0.1 to 0.25 of Iout(max) of the Boost power stage. The inductor ripple current is given by:

$$\mathbf{dI_L = (VDD * D * Ts) / L,}$$

where VDD is the power supply voltage to the Boost converter, D is the duty cycle, Ts is the switching period (1/fs) of the PWM input signal and L is the value of inductor L1.

For example, for the full 6A load current capable of being provided by the EPC7011L7 DUT (GU1), the inductor ripple current should be 0.6 to 1.5Ap-p. So, for the inductor (47uH) implemented on the evaluation board, and assuming a VDD of 12Vdc an output voltage of 25V and a switching frequency of 250kHz, the inductor ripple current will be:

$$dI_L = (12 * 0.568 * 4 * 10^{-6}) / 47 * 10^{-6} = 0.58Ap\text{-}p$$

This analysis is also valuable for determining the peak inductor current (I_{LOAD} + $dI_L/2$) such that the inductor is **NEVER** allowed to enter saturation. For the inductor incorporated on the evaluation board (Wurth 74435584700), the saturation current is 9.5A (for a 10% inductance decrease). This means that for the operating conditions previously stated, the maximum peak inductor current at maximum load is 6 + 1.7/2 = 6.85A, a value well beneath the saturation current level.

Similar analyses can be performed for the desired operating point/conditions by the end-user to ensure safe operation of the evaluation board. If the inductor current ripple is found to be unsuitable with regards to the design target or with respect to the peak current level, then another inductance value from the Wurth WE-HCI series (or another vendor's inductor of similar physical dimensions) may be substituted by the end-user.

EPC7C020 Output Capacitors

The EPC7C020 Evaluation Board is designed with four (4) dual-footprint output capacitor locations: CO1, CO2, CO3 and CO4. Each capacitor location can accept an EIA 1825 ceramic capacitor or a 8.3mm diameter aluminum or organic/conductive polymer electrolytic capacitor (e.g. Chemi-Con HHXF Series) such that end-user may evaluate the performance of a prospective Boost output stage with filter components close to the intended design values and types.

As shipped, the EPC7C020 board comes with Chemi-Con HHXF630ARA470MHA0G conductive polymer capacitors populated in reference designations CO1 and CO2, and with CO3 and CO4 empty (NOPOP).

EPC7011L7 Slowdown Resistors

The EPC7C020 Evaluation Board is designed to include two (2) "slowdown" resistors for the EPC7011L7 IC. Resistor RSD1, on the top-side of the board just adjacent to the left of GU1, is employed to help slow down, or increase, the rise time of the low-side power switch (from SN-to-PGND). Resistor RSD2, on the bottom-side of the board just beneath GU1, is employed to slow down/increase the rise time of the high-side switch. These two resistors are EIA size 0603, and are deployed as 0R0 value on the as-shipped evaluation board. Because the transition times at the switching node are incredibly fast (under 2ns), the resultant rate-of-change-related voltages and currents can be substantial, particularly the voltages from the parasitic loop inductances in the power switching loop (VDD-PGND). There is only so much effective power loop inductance cancellation and power supply bypassing that can be achieved and deployed. So having RSD1 and RSD2 gives the end-user designer two "knobs" that may be turned to alter the switching node transition times to achieve minimum voltage overshoot at the switching node to prevent voltages beyond the de-rating criteria to be impressed upon GU1. Reducing the transition time slew rates also helps reduce EMI in the circuit, particularly radiated emissions.

The values of RSD1 should be in the 18-25 Ohm range and RSD2 should be kept in the 0-50 Ohm range. If higher values are desired, it is recommended that the proposed values be subjected to simulation for switching performance in the planned application configuration using the available PSPICE models.

Thermal "Helpers": TH1 and TH2

The EPC7C020 Evaluation Board is provided with two (2) thermal "helper" locations, populated with aluminum nitride (AlN) thermally-conductive, but electrically isolated, elements TH1 and TH2. These two helpers allow the heat generated by the EPC7011L7 IC (GU1) to be spread over a larger physical area, thus reducing the apparent junction-to-case (Rth(j-c)) thermal resistance of the IC. Components TH1 and TH2 are located just above (to the "north") of GU1. These components may be left as deployed in the as-shipped evaluation board, one or the other may be removed to observe the thermal effects or both may be removed – and additional EIA 0805 bypass capacitors may be substituted to help reduce the inevitable leading edge switching spike that is attendant with the quick switching node transition times.

Blocking Diode: D5

The EPC7C020 Evaluation Board is provided with a blocking diode location, D5. This diode PCB shape is provisioned for an EIA SMA-123FL packaged-diode. This diode location is not-populated (NOPOP) on the as-shipped evaluation board. Diode D5 should be populated to help reduce dead-time-related power losses, as the Vf of a Schottky diode is less than the Vsd of the eGaN HEMT synchronous blocking transistor in the EPC7011L7 IC.

EPC7C020 Evaluation Board Minimum and Maximum Ratings

The EPC7C020 is rated for the following operation:

VDD: 5Vdc to 40Vdc

VOUT(Max): 40Vdc

ILOAD: 0A minimum to 6A maximum.

VBIAS: 12.0Vdc (+/-0.5Vdc),

PWM IN: 0-3.0V minimum/0-5.0V maximum/200kHz to 1.5MHz/95% duty cycle maximum.

Recommended Test Equipment Connections: AC Switching Operation

Figure 7 shows the recommended connection to/from the Evaluation Board for switching operation.

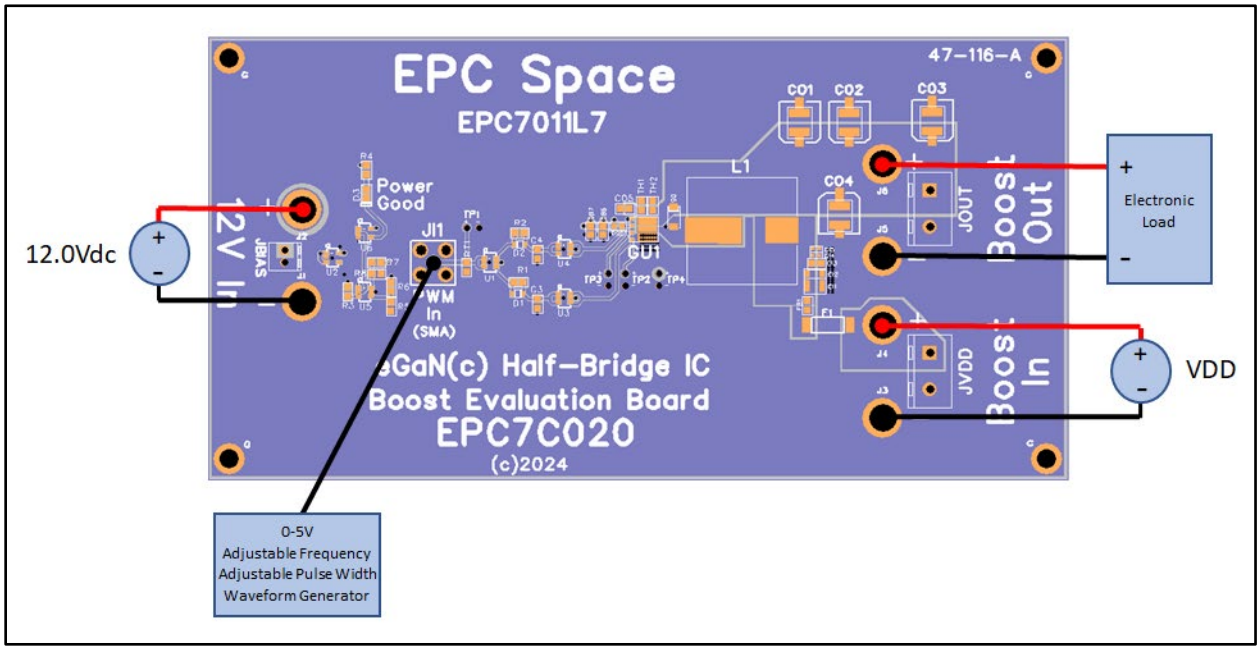

Figure 7. *EPC7C020 Evaluation Board Test Equipment Connections: AC Switching Operation.*

It is recommended that the connections to the EPC7C020 Eval. Board from the VBIAS (12.0V) and VDD power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable.

Recommended Test Equipment: AC Switching Operation

1.) The following test equipment is recommended to properly evaluate the EPC7C020 Eval. Board as shown in Figure 5:

0-50V, 10A adjustable DC power supply;
0-20V, 100mA adjustable lab power supply set to 12.0Vdc;
50V/10A electronic load;
0-1.5MHz, 0-5V, adjustable duty cycle signal generator;
500MHz two channel oscilloscope;
Two 10:1 passive oscilloscope probes configured with 0.100” spacing between probe tip and ground;
Quantity 6 – 12” to 18” banana plug-to-banana plug cables.

AC Switching Operation Test Procedure

With the evaluation board connected to the test equipment as shown in Figure 7, the switching node (SN) waveform may be monitored using the following test sequence:

1.) Insert a 0.100” spaced probe/ground into test point TP4, observing the proper polarity for ground;

2.) Apply the desired PWM signal;

3.) Turn on VBIAS;

4.) Adjust the electronic load to the desired output current value and enable the output;

5.) Turn on VDD.

When the Boost evaluation circuit is ON and running, the load current (ILOAD) and the PWM duty cycle may be adjusted to obtain the desired value of VLOAD/VOUT.

The resultant SN waveform may be captured for review/analysis.

NOTE: **NEVER** adjust the PWM frequency while the EPC7C020 Boost circuit is ON and running. Damage/destruction of the FBS GAM02 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks on the evaluation board.

Recommended Test Equipment Connections: Conversion Efficiency

Figure 8 shows the recommended connection to/from the Evaluation Board for switching operation.

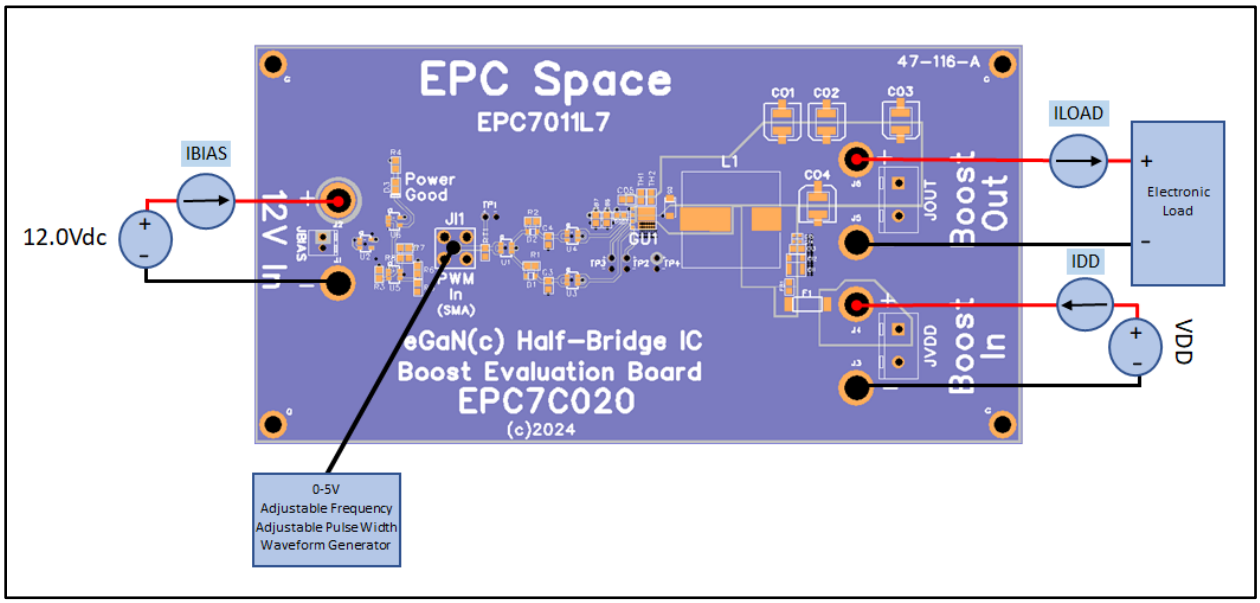

Figure 8. *EPC7011L7 Boost Evaluation Board Test Equipment Connections: Conversion Efficiency.*

It is recommended that the connections to the EPC7C020 Eval. Board from the VBIAS (12.0V) and VDD power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable. Voltages VDD, VBIAS and VLOAD should be monitored/measured at the associated banana jacks on the board.

Recommended Test Equipment: Conversion Efficiency

1.) The following test equipment is recommended to properly evaluate the EPC7C020 Eval. Board as shown in Figure 6:

0-50V, 10A adjustable DC power supply;
0-20V, 100mA adjustable lab power supply set to 12.0Vdc;
50V/10A electronic load;
0-1.5MHz, 0-5V, adjustable duty cycle signal generator;
500MHz two channel oscilloscope;
Two 10:1 passive oscilloscope probes configured with 0.100” spacing between probe tip and ground;
Quantity 3 – Precision digital voltmeters (one to monitor VDD, VBIAS and the load voltage, VLOAD);
Quantity 3 – Precision digital ammeters (one to monitor IDD, IBIAS and the load current, ILOAD);
Quantity 15 – 12” to 18” banana plug-to-banana plug cables.

Conversion Efficiency Test Procedure

With the evaluation board connected to the test equipment as shown in Figure 8, the conversion efficiency of the Boost output stage may be determined at multiple operating points.:

1.) Apply the desired PWM signal, frequency and duty cycle;

3.) Turn on VBIAS;

4.) Adjust the electronic load to the desired output current value and enable the output;

5.) Turn on VDD.

When the Boost evaluation circuit is ON and running, the load current (ILOAD) may be increased in small increments and the PWM duty cycle may be adjusted to obtain the desired value of VLOAD/VOUT at each operating point. A most accurate efficiency is obtained if VDD is adjusted to the same value at each value of load current and then the PWM duty cycle is subsequently adjusted to desired value of VLOAD/VOUT.

The conversion efficiency (η) at each operating point is defined as:

$$\eta = (VLOAD * ILOAD) / [(VDD * IDD) + (VBIAS * IBIAS)]$$

NOTE: **NEVER** adjust the PWM frequency while the EPC7C020 Boost circuit is ON and running. Damage/destruction of the EPC7011L7 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks on the evaluation board.

BIN-TIN and TIN-BIN Dead Time Typical Waveforms

The waveform shown in Figure 9 is typical of the BIN-TIN and TIN BIN dead times for C1 = C2 = 15pF. Logic input BIN is the yellow trace and TIN is blue, at 50% duty cycle:

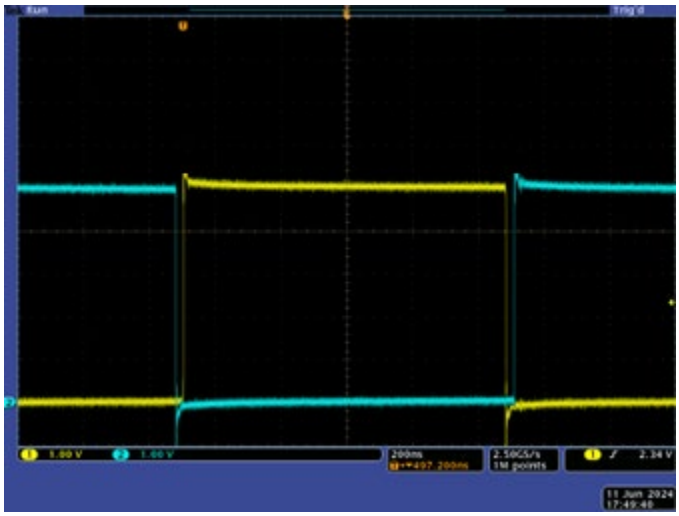

Figure 9. *EPC7C020 Evaluation Board BIN-TIN and TIN BIN Logic Input Dead Time.*

Typical Switching Node (SN) Waveform

The waveform shown in Figure 10 is typical of the switching node for Eval. Board operation at VDD = 20V, Vout = ~40V, D = 50%, fs = 300kHz and ILOAD = 1.5A:

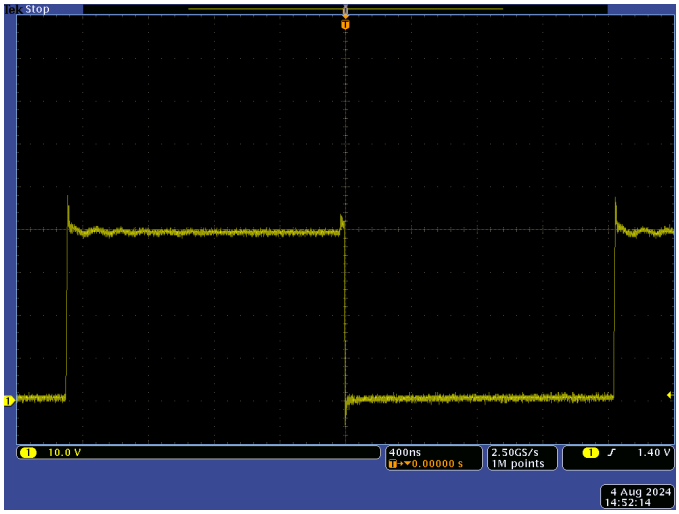

Figure 10. *EPC7011L7 Boost Evaluation Board Typical Switching Node Waveform.*

The waveform shown in Figure 11 is typical of the switching node rising transition time for the evaluation board operation under the same conditions as in Figure 10:

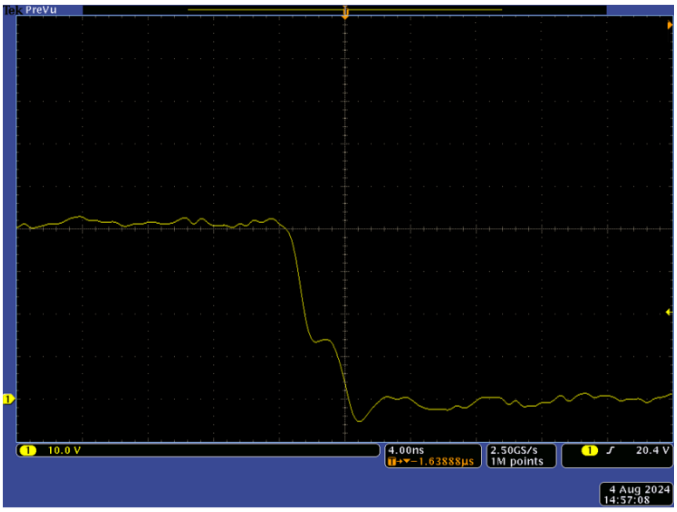

Figure 11. *EPC7C020 Boost Evaluation Board SN Typical Rise Time Waveform.*

The waveform shown in Figure 12 is typical of the switching node falling transition time for the evaluation board operation under the same conditions as in Figure 10:

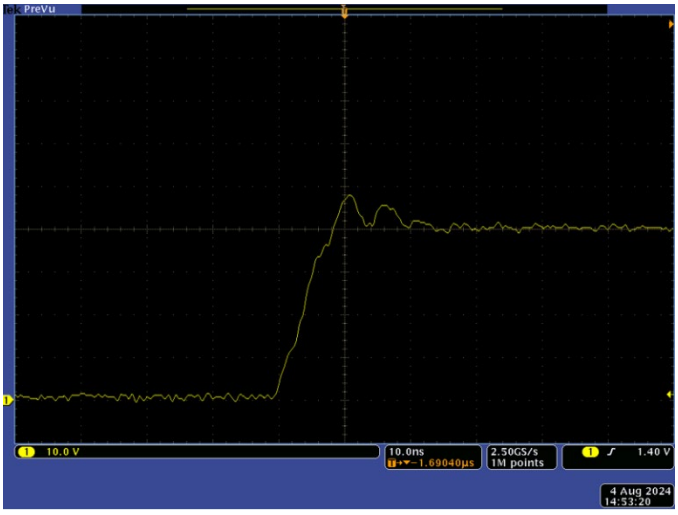

Figure 12. *EPC7C020 Boost Evaluation Board Typical Fall Time Waveform.*

Typical Conversion Efficiency Graphs

The graph shown in Figure 13 is typical of the EPC7C020 evaluation board conversion efficiency at switching frequencies of 200kHz and 300kHz. The duty cycle was adjusted to obtain a 36.0V output for each load current set point for an input voltage of 15Vdc:

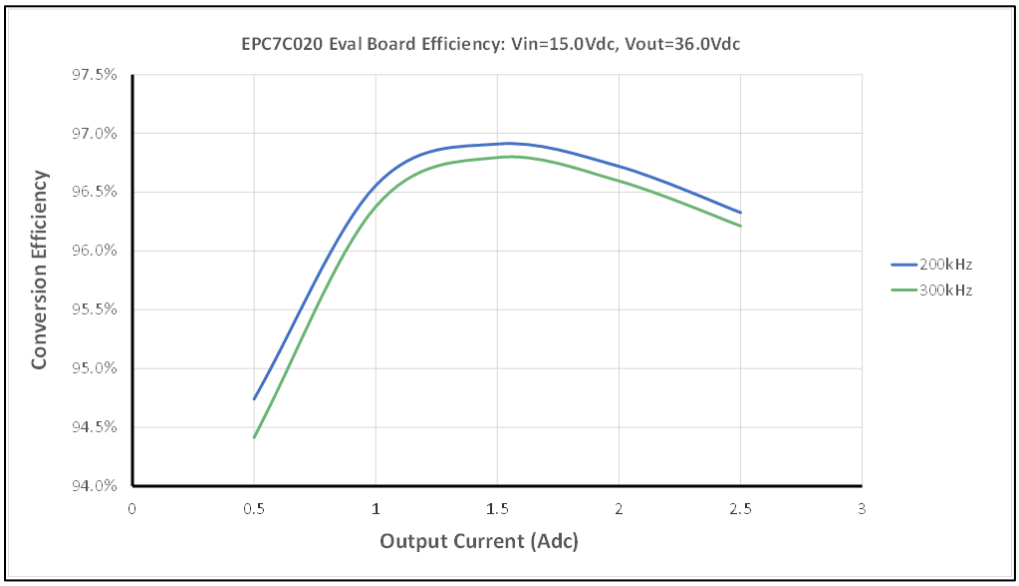

Figure 13. *EPC7011L7 Boost Evaluation Board Typical Conversion Efficiency: Vin = 15V, Vout = 36V and fs = 200kHz and 300kHz.*

The graph shown in Figure 14 is typical of the EPC7C020 evaluation board conversion efficiency at switching frequencies of 300kHz and 500kHz for an input voltage of 20V and a duty cycle of 50%:

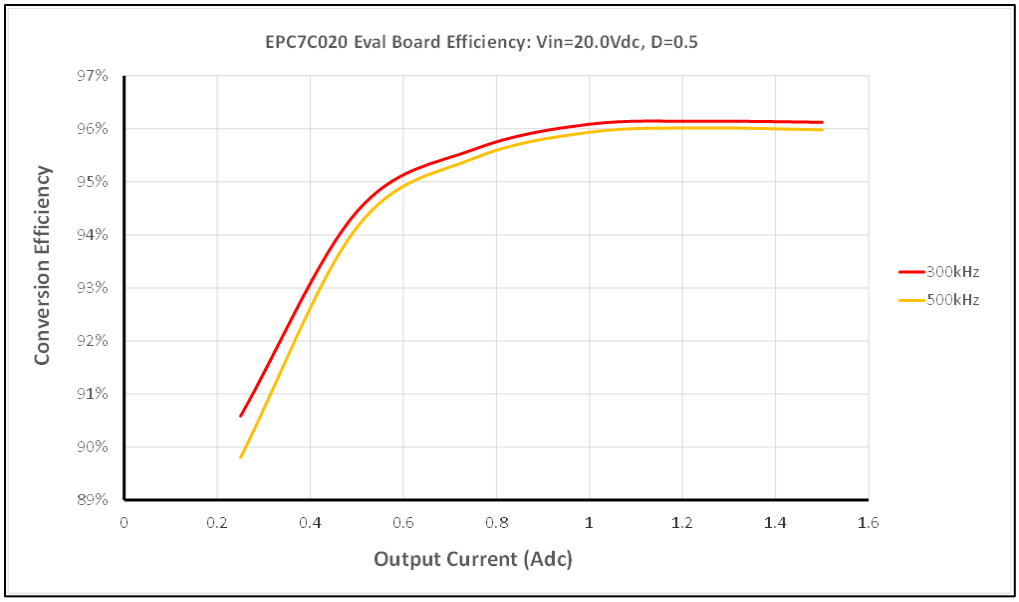

Figure 14. *EPC7011L7 Boost Evaluation Board Typical Conversion Efficiency: Vin = 20V, Vout = ~40V and fs = 300kHz and 500kHz.*

The graph shown in Figure 15 is typical of the EPC7C020 evaluation board conversion efficiency at switching frequencies of 300kHz and 500kHz for an input voltage of 10V and a duty cycle of 75%:

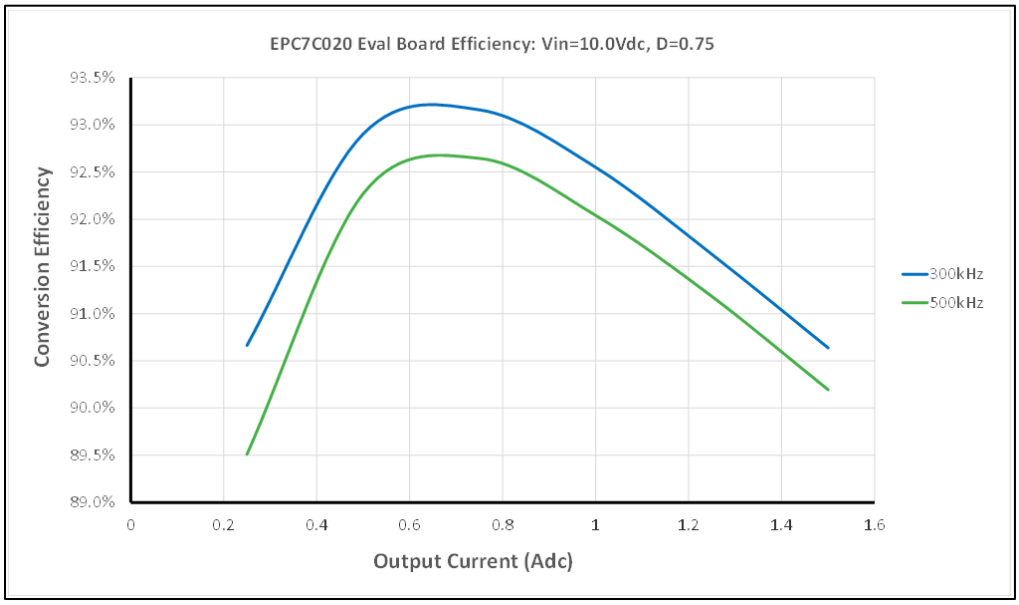

Figure 15. *EPC7011L7 Boost Evaluation Board Typical Conversion Efficiency: Vin = 10V, Vout = ~40V and fs = 300kHz and 500kHz.*

Optimization of Conversion Efficiency Performance

No attempt has been made to optimize the conversion efficiency performance of the EPC7C020 EPC7011L7 Boost evaluation board. The board was, however, optimized for switching performance and to provide the best switching waveforms in terms of minimizing stray inductances in the power loop to prevent transient overshoots at the switching node and VDD.

Because the evaluation board was intended to be used over a wide range of input and output voltages, load currents and switching frequencies, there could be no “optimized” set of components used for all possible applications to achieve the highest possible conversion efficiency. As such, optimization of the evaluation board for a particular customer end-use application is left to the designer who is evaluating this board.

The end-user is invited to change component values (inductor L1 and/or capacitors CO1-CO4) or cut-in their own planned components for their design using the EPC7C020 board as their starting point. It provides a convenient vehicle for achieving the desired performance results in a very short amount of time!

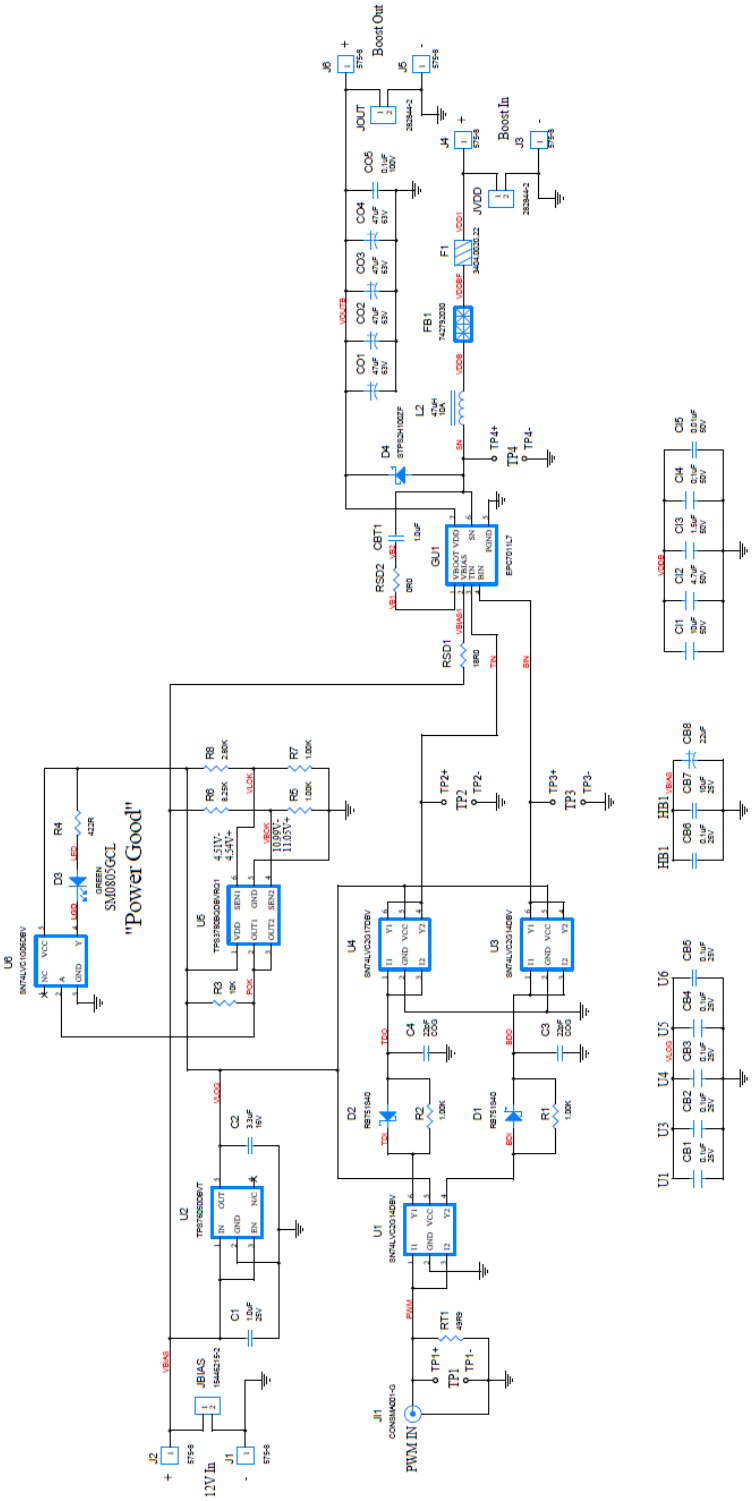

Figure 16. *EPC7C020/EPC7011L7 Boost Evaluation Board Schematic Diagram.*

[**NOTE:** The above schematic is recognized and understood to be an eye-test for the reader due to its low resolution, and a higher-resolution PDF version may be obtained upon request from EPC Space.]

EPC7C020 / EPC7011L7 Boost Evaluation Board BOM

The BOM for the EPC7C020 Boost Evaluation Board is shown in Table III.

Table III. EPC7C020/EPC7011L7 Boost Evaluation Board Bill of Materials.

Master BOM							
Item	Quantity	Ref. Des.	Description/Value	Mfgr.	Mfgr. P/N	Size/Package	Notes/Comments
1	6	J1,J2,J3,J4,J5,J6	Staking Banana Jack, Uninsulated	Keystone	575-8	0.208" Dia. Hole	Install at each 0.208" diameter hole.
2	2	C1,CBT1	1.0uF/50V/X7R/10%/0805 Ceramic Capacitor	AVX/Kyocera	08055C105K4T4A	C0805	1uF/50V
3	1	C2	3.3uF/25V/X7R/10%/0805 Ceramic Capacitor	TDK	C2012X7R1E335K125AB	C0805	3.3uF/25V
4	2	C3,C4	15pF/50V/C0G/2%/0805 Ceramic Capacitor	Kemet	C0805C150F5GACAUTO	C0805	15pF/50V
5	7	CB1,CB2,CB3,CB4,CB5,CB6,CO5	0.1uF/50V/X7R/10%/0805 Ceramic Capacitor	Kemet	C0805C104K5RECAUTO	C0805	0.1uF/50V
6	1	CB7	10uF/25V/X7R/10%/0805 Ceramic Capacitor	Murata	GRM21BZ71E106KE15L	C0805	10uF/25V
7	1	CB8	22uF/25V/Tantalum/10%/IC Case Tantalum SMT Capacitor	Kemet	T9SC226K025R0400	TANT_C	22uF/25V. Observe polarity when placing.
8	1	CI1	10uF/100V/X7R/10%/1210 Ceramic Capacitor	TDK	C3225X7R2A106K250AC	C1210	10uF/100V
9	1	CI2	4.7uF/100V/X7R/10%/1210 Ceramic Capacitor	Kemet	C1206C475K5RACAUTO7210	C1206	4.7uF/100V
10	1	CI3	1.0uF/100V/X7R/10%/0805 Ceramic Capacitor	AVX/Kyocera	08051C105K4T2A	C0805	1uF/100V
11	1	CI4	0.1uF/100V/X7R/10%/0603 Ceramic Capacitor	AVX/Kyocera	KAM15BR72A104KT	C0603	0.1uF/100V
12	1	CI5	0.01uF/100V/X7R/10%/0603 Ceramic Capacitor	AVX/Kyocera	06031C103K4T2A	C0603	0.01uF/100V
13	2	CO1,CO2	47uF/63V/Alum. Dig. Polymer/20%/8mm x 10mm SMT Capacitor	Chemi-Con	HHXF630ARA470MHA0G	HHXF630ARA470MHA0G	47uF/63V. Observe polarity when placing.
14	2	D1,D2	0.12A/40V/SOD-323 Schottky Diode	ON Semi	RB751V40T1G	SOD-323	Observe polarity/orientation when placing.
15	1	D3	568nm Green Water Clear/0805 Package LED	Bivar	SM0805GCL	D0805	Observe polarity/orientation when placing.
16	NOPOP	D4	2A/100V/SOD-123Flat Schottky Diode	ST	STPS2H100ZF	SOD123Flat	NOPOP
17	1	F1	8A/12.5 milliohms/Fast Blow/2-SMD SMT Fuse	Schurter	3404.0020.22	2-SMD	
18	1	FB1	10A/20 Ohm/0.003 Ohms Ferrite Bead	Wurth	742792030	R0805	
19	1	GU1	EPC7011 Half-Bridge IC/L7 Package	EPC Space	EPC7011L7	EPCSL7	
20	1	J1	SMA/Vertical/50 Ohms/Brass-Gold/SMT	Linx Tech.	CONSMA001-G	CONSMA001-G	
21	1	JBIAS	2 Position/2.54mm/150V/Fixed Terminal Block	TE	1546215-2	1546215-2	
22	1	JVDD_JOUT	2 Position/7.5mm/300V/Fixed Terminal Block	TE	282844-2	282844-2	
23	1	L1	9A/4.7uH Power Inductor/19.2 milliohms/22.5mm x 22mm	Wurth	7443556470 0	7443556470 0	
24	1	R4	422R/1%/0805/Thick Film Chip Resistor	Vishay	CRCW0805422RFKEA	R0805	422R
25	1	RSD1	18R0/1%/High Power/0603 Thick Film Jumper Chip Resistor	Vishay	CRCW060318R0FKEAHP	R0603	18R0/HP
26	1	RSD2	0R0/1%/0603 Thick Film Jumper Chip Resistor	Vishay	RCC0603000020EA	R0603	0R0
27	4	R1,R2,R5,R7	1.0K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08051K00FKEA	R0805	1.0K
28	1	R3	10.0K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW080510K0FKEA	R0805	10.0K
29	1	R6	8.25K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08058K25FKEA	R0805	8.25K
30	1	R8	2.80K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW080528K0FKEA	R0805	2.80K
31	1	RT1	49R9/1%/0805 Thick Film Chip Resistor	Panasonic	ERJ-P06F49R9V	R0805	
32	2	TH1,TH2	AlN Thermal "Helper" Chip/0.025" th/Wraparound Term/0805	IMS	BGR-0805WA	R0805	
33	1	U4	Dual Schmitt-Trigger Buffer/Little Logic/1.65-5.5V/LVC/SOT-23-6	TI	SN74LVC2G17DBVR	SOT-23-6	Observe polarity/orientation when placing.
34	1	U2	5V/50mA LDO Regulator/6.5V/SOT-23-5	TI	TPS76050DBVT	SOT-23-5	
35	1	U1,U3	Dual Schmitt-Trigger Inverter/Little Logic/1.65-5.5V/LVC/SOT-23-6	TI	SN74LVC2G14DBVR	SOT-23-6	Observe polarity/orientation when placing.
36	1	U5	Dual Voltage Supervisor/Open Drain/5V/1%/SOT-23-6	TI	TPS3780B0QDBVRQ1	SOT-23-6	Observe polarity/orientation when placing.
37	1	U6	Single Open-Drain Inverter/Little Logic/1.65-5.5V/LVC/SOT-23-5	TI	SN74LVC1G06DBVR	SOT-23-5	
38	6	Hardware	Spacer/Hex/Aluminum/6-32/2-1/8" Length	Essentra	14HTSP008	N/A	
39	6	Hardware	Screw/6-32/Nylon/Pound head/Slotted/0.5" Length	Essentra	010632R050	N/A	
40	1	PCB	5.62" x 3.72" x 0.063", 6 Layer FR-4 PCB, Double-Sided	4PCB.com	47-101-A	N/A	

Printed Circuit Board and Layout Details

The printed circuit board (PCB) for the EPC7C020 EPC7011L7 Boost Evaluation Board is constructed with four layers. The PCB is 6.94" x 3.59" and is 0.063" thick. The outer layers are 2 oz/in^2 and the inner layers are 1 oz/in^2 copper etch. All electronic components are SMT-packages and all connectors are through-hole.

The individual Gerber layers for the PCB are shown in Figures 17 to 25, following:

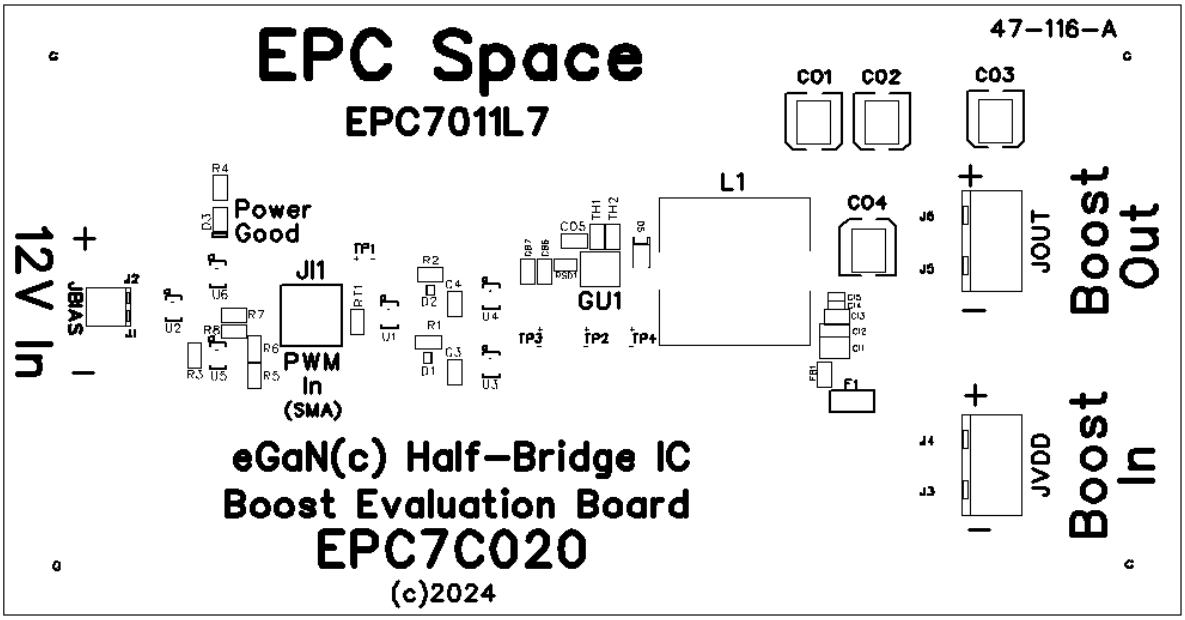

Figure 17. *EPC7C020/EPC7011L7 Boost Evaluation Board Top Silkscreen.*

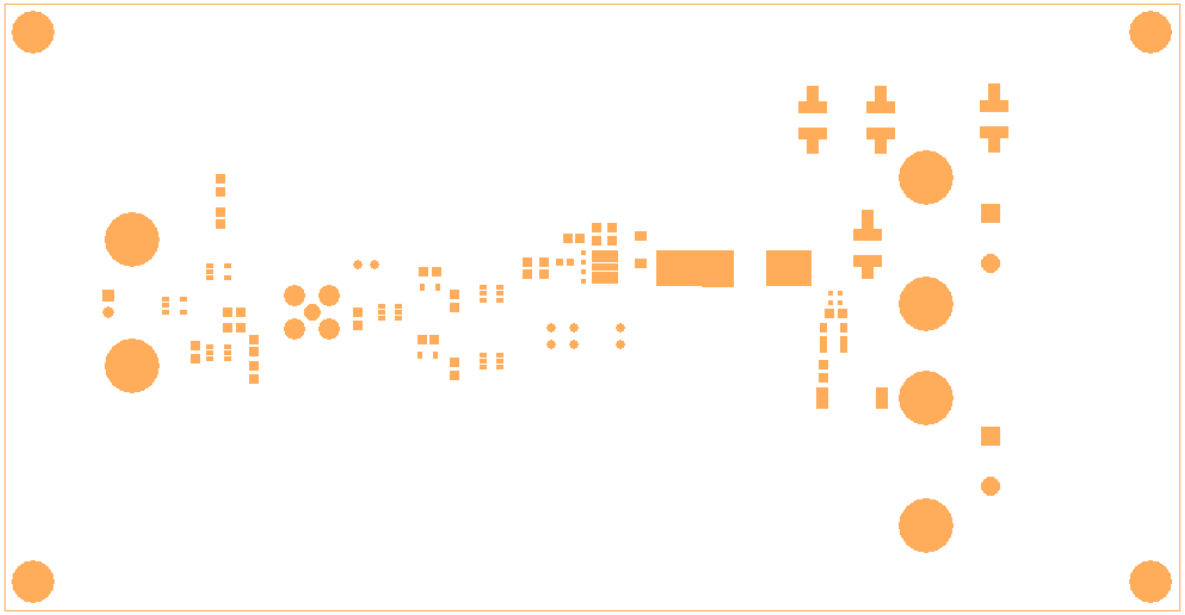

Figure 18. *EPC7C020/EPC7011L7 Boost Evaluation Board Top Solder Mask.*

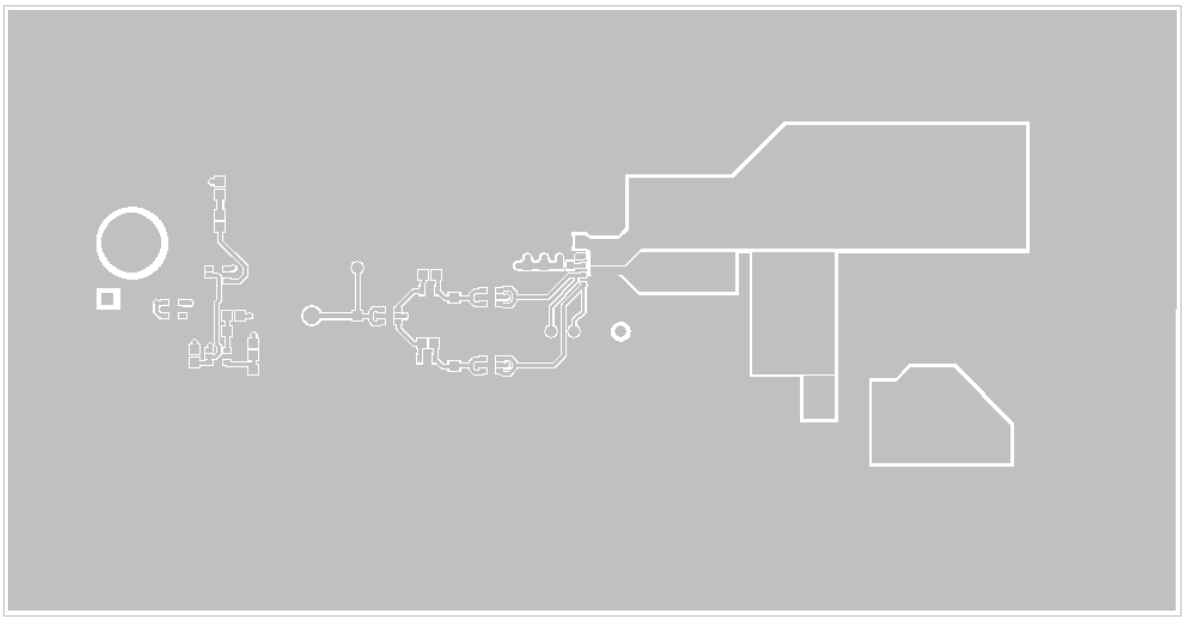

Figure 19. *EPC7C020/EPC7011L7 Boost Evaluation Board Top Copper Etch (2 oz).*

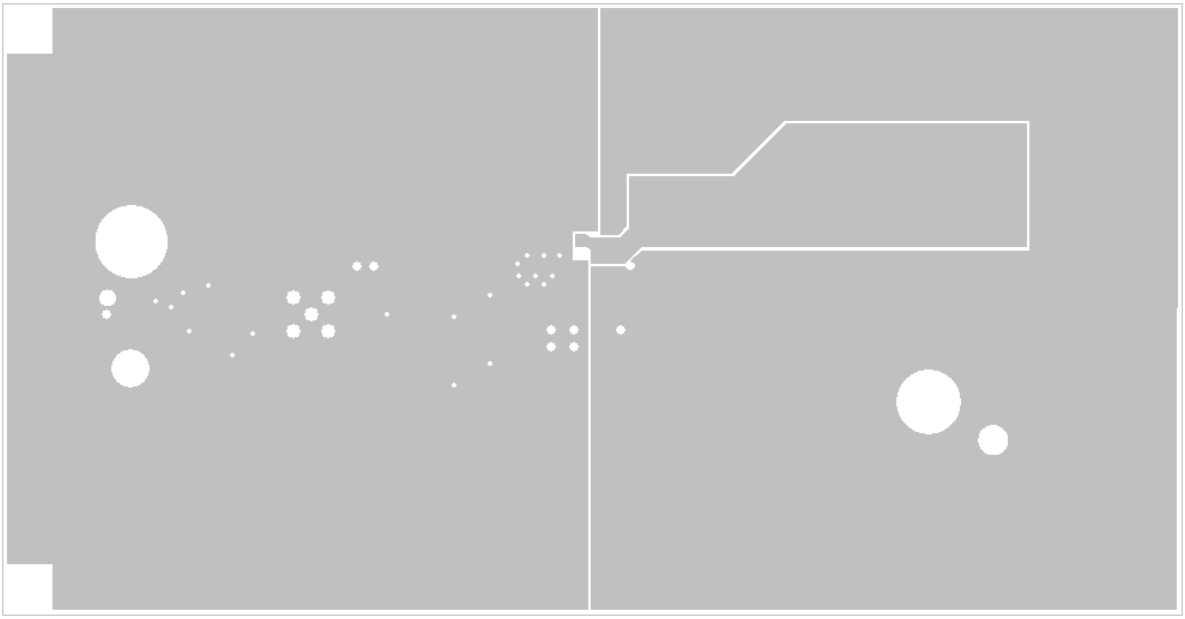

Figure 20. *EPC7C020/EPC7011L7 Boost Evaluation Board Inner Layer 1 Copper Etch (1 oz).*

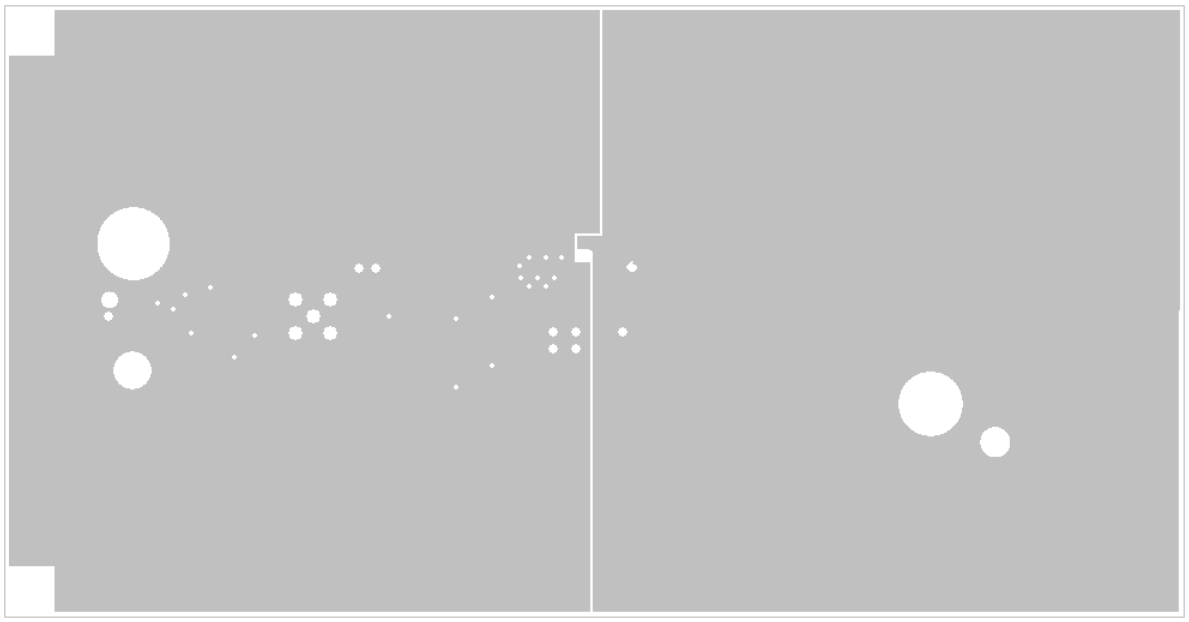

Figure 21. *EPC7C020/EPC7011L7 Boost Evaluation Board Inner Layer 2 Copper Etch (1 oz).*

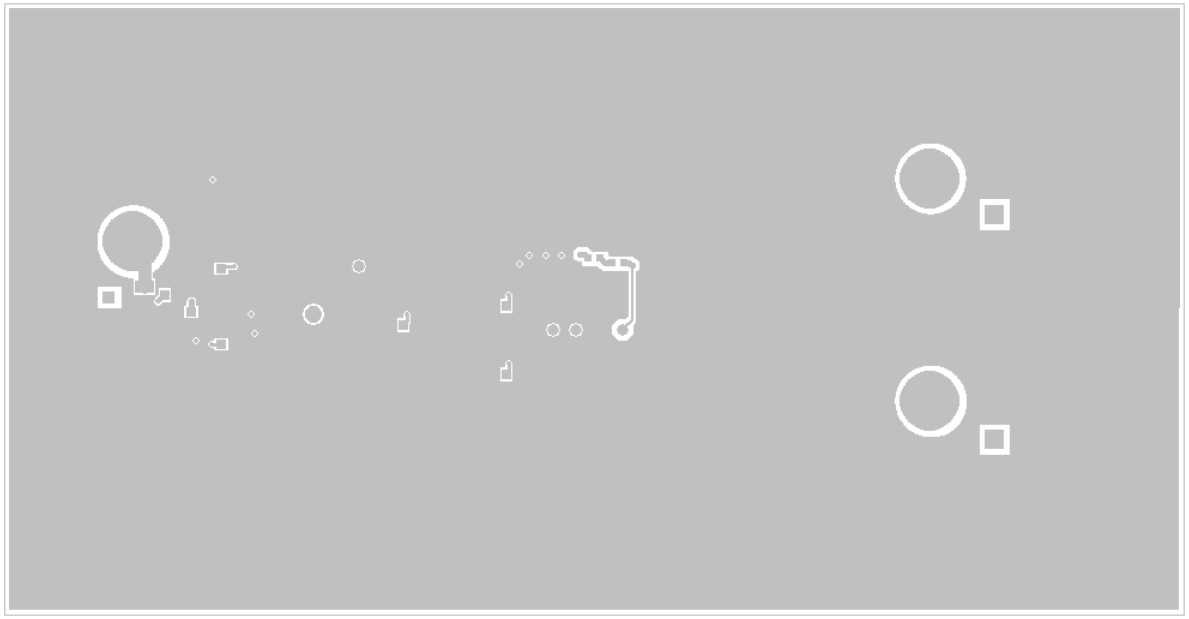

Figure 22. *EPC7C020/EPC7011L7 Boost Evaluation Board Bottom Copper Etch (2 oz).*

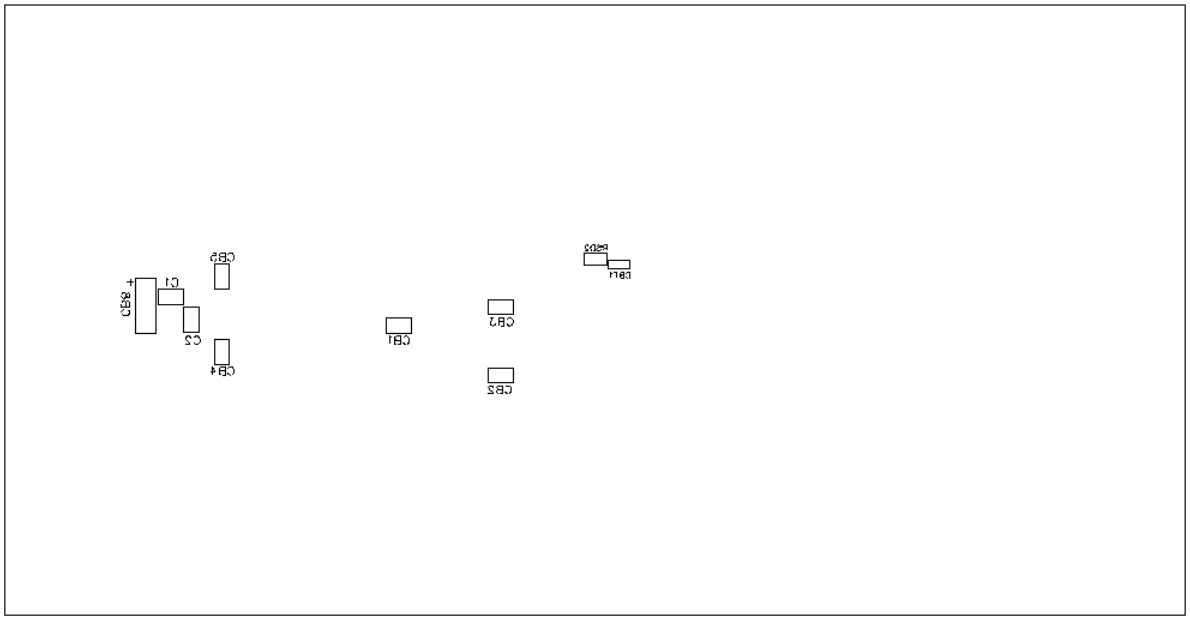

Figure 23. *EPC7C020/EPC7011L7 Boost Evaluation Board Bottom Silkscreen.*

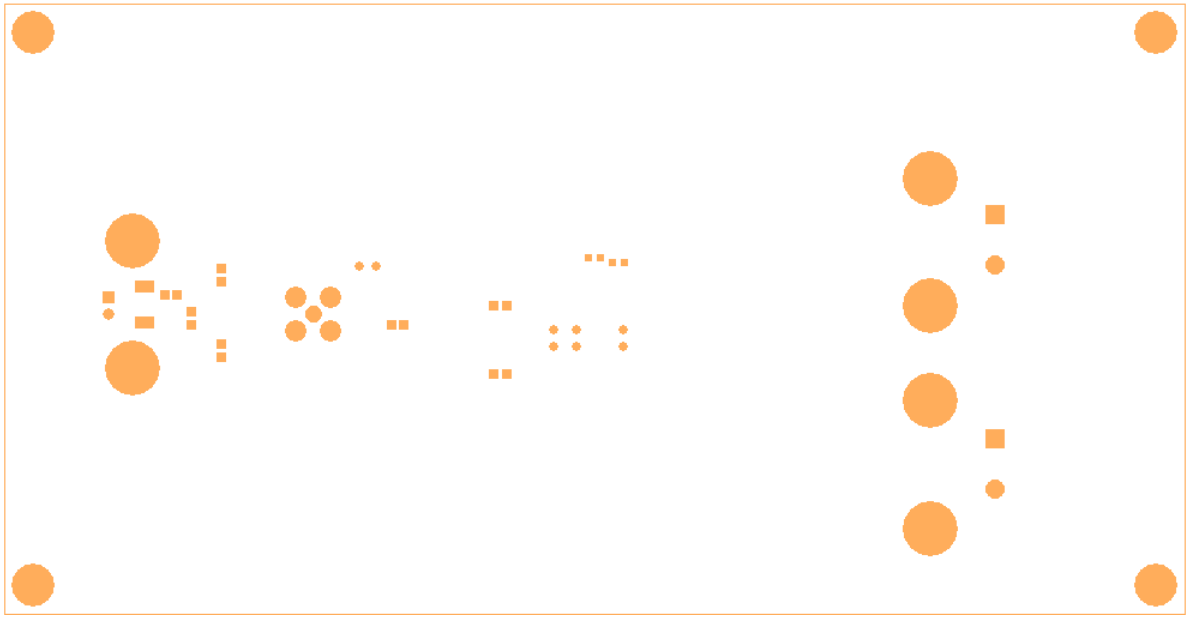

Figure 24. *EPC7C020/EPC7011L7 Boost Evaluation Board Bottom Solder Mask.*

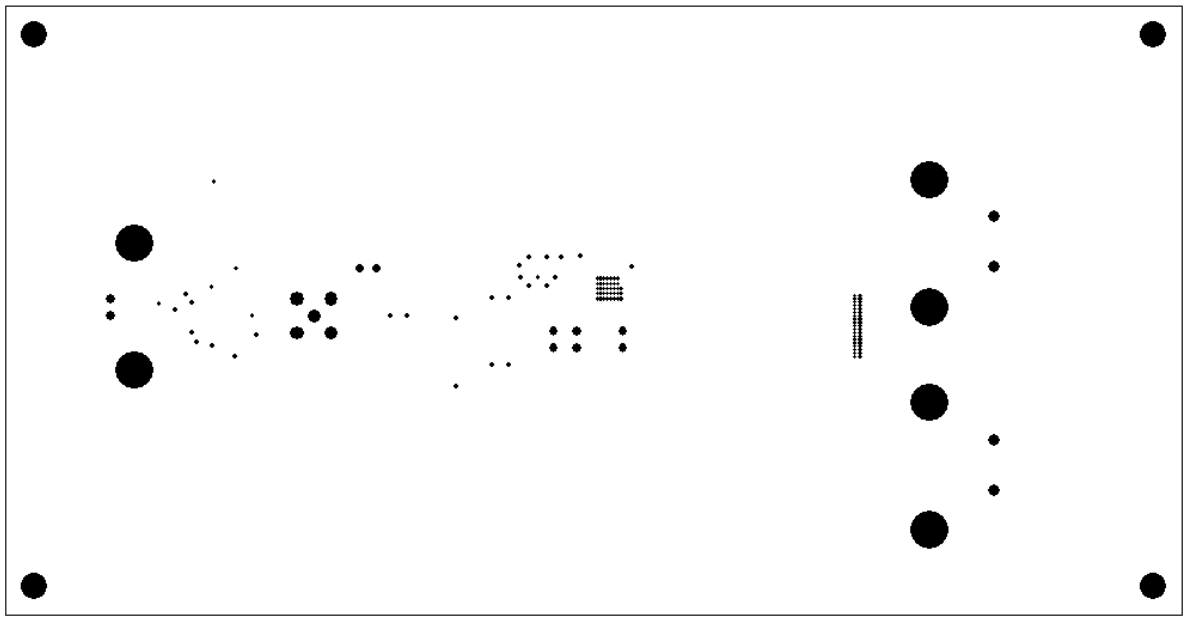

Figure 25. *EPC7C020/EPC7011L7 Boost Evaluation Board Drill Pattern.*

NOTES:

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Revisions:

Revision	Date	Status
PR	8/5/2024	Pre-Release
--		Release
A		Revision A

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