ATTENTION
ELECTROSTATIC
SENSITIVE DEVICE

Proper ESD precautions should be employed when handling the EPC7C00x series demo boards to prevent damage to the components installed on the board.

Introduction

This document describes the recommended connection of the EPC7C002 demo board to power supplies and monitoring instruments for proper operation for the evaluation of the switching performance of the EPC Space single, low-side gate driver driving an associated power output HEMT.

This document also provides typical switching performance, the schematic of the evaluation board and the layout of the board in the form of layer-by-layer Gerber rendering of the evaluation printed circuit board.

Evaluation PCB Photograph

Figure 1a shows the top view and Figure 1b shows the bottom view of the demo board. These pictures illustrate the component placements, power and input signal connections and the numerous test points available for monitoring by the end-user.

Description of Test Points

The description of each test point on the EPC7C002 demo board is found in Table 1.

Each set of test points (signal to be measured as indicated by "+", and ground as indicated by "-") have the physical spacings shown in Table 1 so as to facilitate easy oscilloscope probing by the end-user.

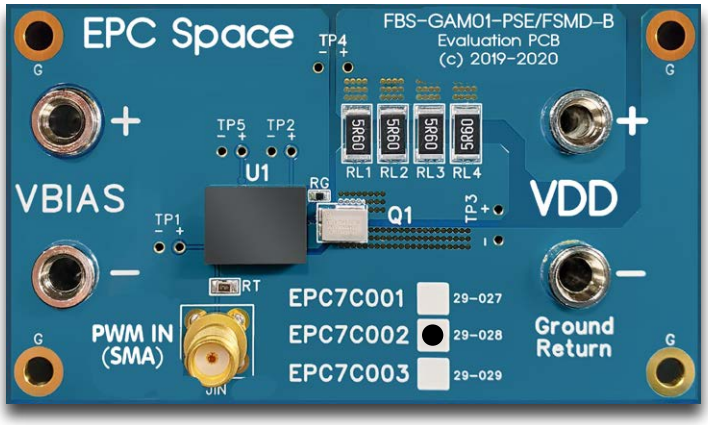


Figure 1a. EPC7C002 Demo Board (Top View)

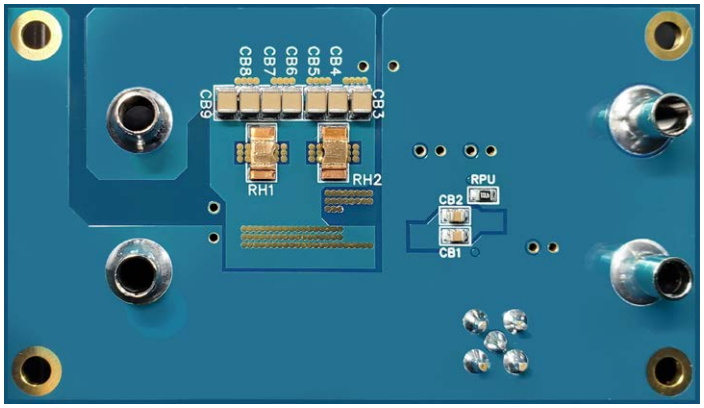


Figure 1b. EPC7C002 Demo Board (Bottom View)

Table 1. EPC7C002 Demo Board Test Point Identification

Test Point	+/- Spacing (in.)	Parametric Measurement Location
TP1	0.100	PWM Input Signal Monitor
TP2	0.100	Q1 Gate Signal Monitor
TP3	0.150	Q1 Drain Signal Monitor
TP4	0.150	V_{DD} Signal Monitor
TP5	0.100	PG (Power Good) Monitor

IMPORTANT NOTE: The "–" side of each test point is connected to the ground potential (i.e. 0 V_{DC}) of the Demo Board. ALWAYS make sure that the ground connection to the oscilloscope is connected to this point when power is applied to the board as damage may occur to the oscilloscope, the demo board or BOTH.

Recommended Test Equipment Connections

Figure 2 shows the recommended connection to/from the EPC7C002 Demo Board.

It is recommended that the connections to the Demo Board from the V_{BIAS} (5 V) and V_{DD} power supplies be made with banana plug-to-banana plug cables. The connection from the pulse/frequency generator should be made via an SMA (board)-to-BNC (generator) cable.

Recommended Test Equipment

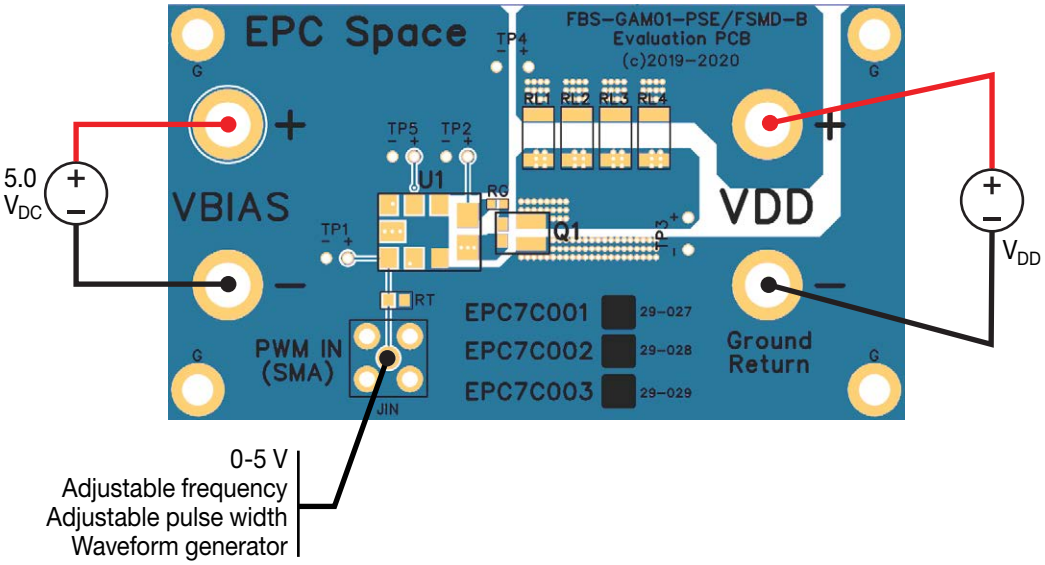
The following test equipment is recommended to properly evaluate the EPC7C002 demo board:

- 0-100 V, 1 A adjustable DC power supply
- 0-10 V, 100 mA adjustable lab power supply set to 5 Vdc
- 0-1 MHz, 0-5 V, adjustable duty cycle signal generator
- 500 MHz two channel oscilloscope
- Two 10:1 passive oscilloscope probes configured with 0.100" spacing between probe tip and ground

V_{DD} Settings and Load Resistor Values

There are three versions of the demo board: the EPC7C001 is a 40 V version that utilizes an FBG04N30 power HEMT for Q1; the EPC7C002 is a 100 V version that utilizes the FBG10N30 HEMT; and the EPC7C003 is a 200 V version that utilizes the FBG20N18 HEMT.

The demo board is configured to observe the switching performed at one-half the maximum rated BV_{DSS} of the HEMT used for Q1. The load resistors (RL1 through RL4 in Figure 2) are selected to provide approximately one-half the maximum rated load current draw at this one-half de-rated V_{DD} supply voltage. The operating V_{DD} level versus HEMT used for Q1 versus the resultant load current is shown in Table 2.



IMPORTANT NOTE: Due to the physical size and power rating limitations of the load resistors, it is required that the duty cycle of the ON-state test pulse provided to the FBS-GAM01P-PSE driver be limited to 2%, maximum, of the PWM switching frequency, for any frequency supplied to the Demo Board.

Figure 2. EPC7C002 Demo Board Test Equipment Connections

Table 2. EPC7C002 Demo Board Load Resistance vs. Drain Current

EPC Space P/N	Q1 HEMT	V_{DD} (V)	Load Resistance (Ω)	I_D (A)
EPC7C002	FBG10N30	50	3.25	15.4

Typical Switching Performance

The following switching performance was obtained for the Demo Board at 200 kHz and 1% duty cycle. The parameters ON delay time ($t_{d(ON)}$), rise time (t_r), OFF delay time ($td_{(OFF)}$) and fall time (t_f) are shown for each HEMT voltage version. All the following oscilloscope captures were obtained via TP1 (PWM In, yellow) and TP3 (Q1 Drain, blue).

FBG10N30, V_{DD} = 50 V_{DC}

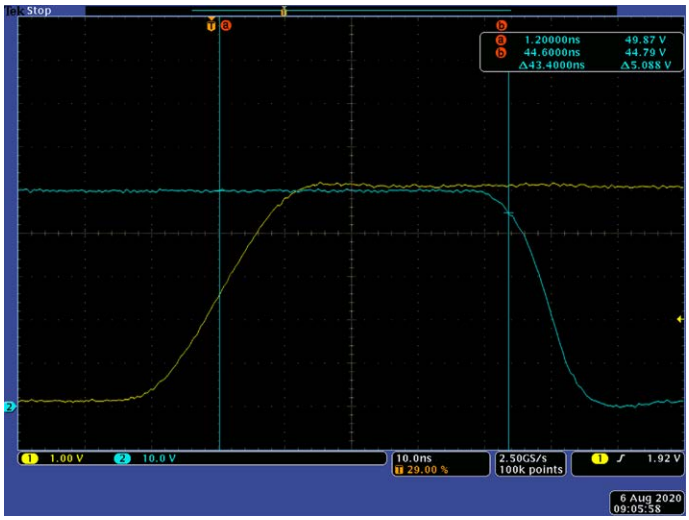


Figure 3. FBG10N30 $t_{d(ON)}$

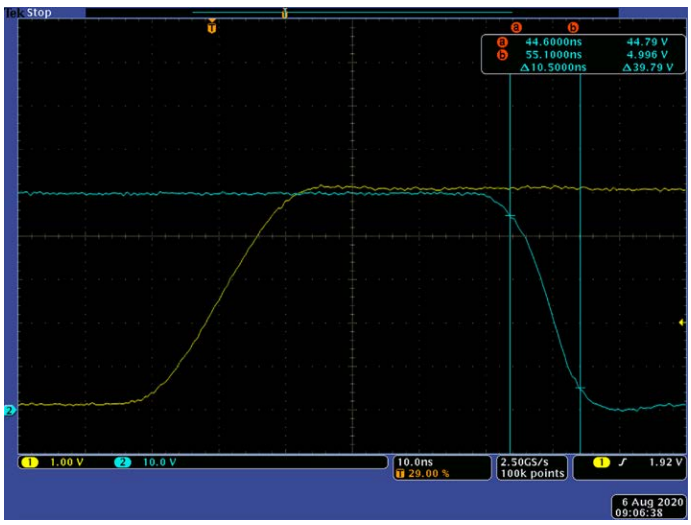


Figure 4. FBG10N30 t_r

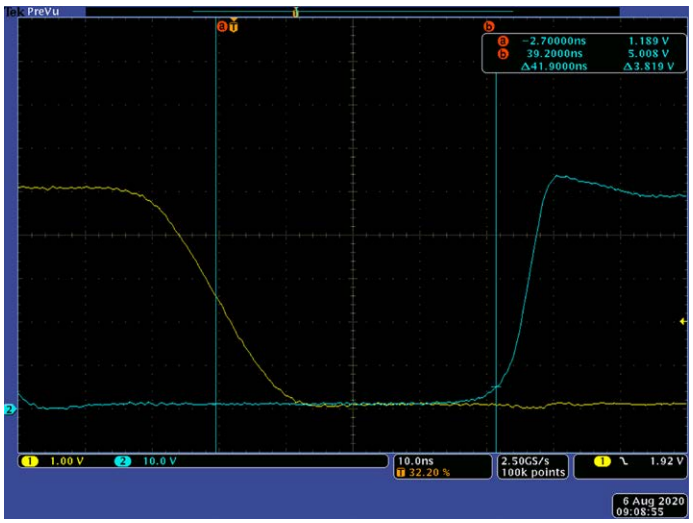


Figure 5. FBG10N30 $t_{d(OFF)}$

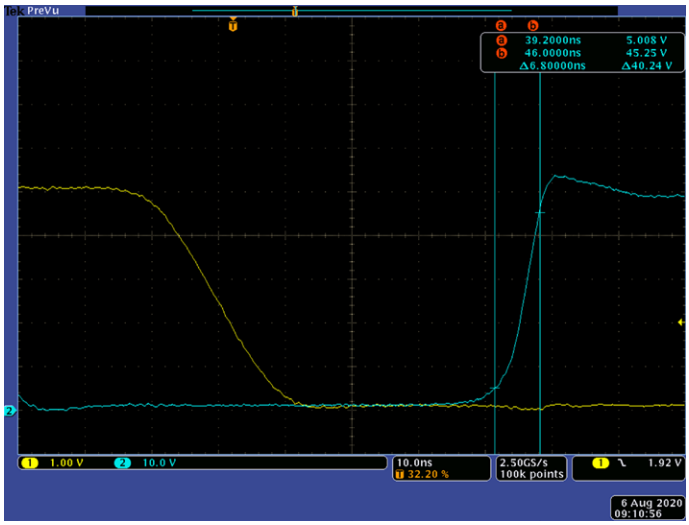


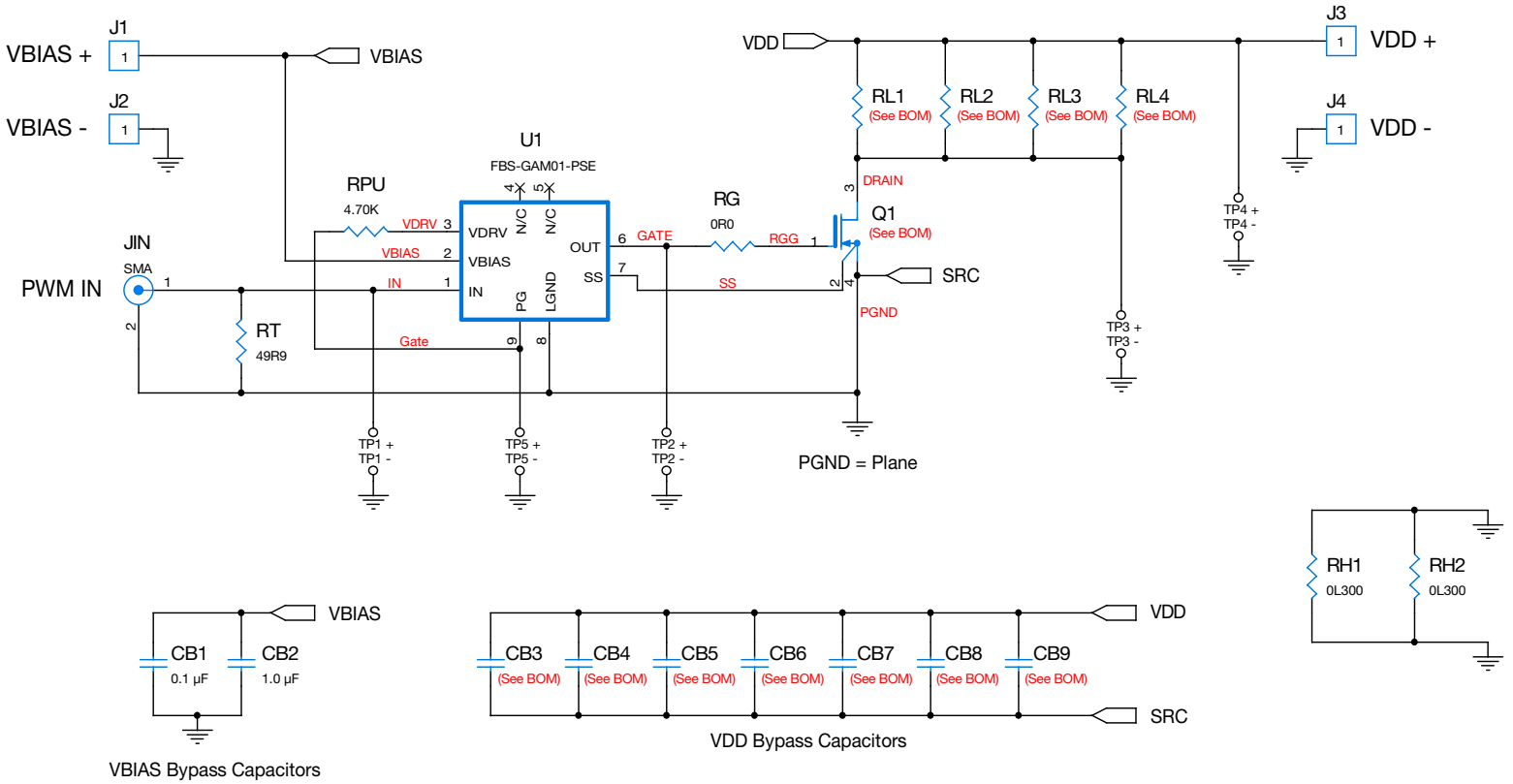
Figure 6. FBG10N30 t_r

The typical switching performance obtained is summarized in Table 3.

Table 3. Switching Performance Summary

EPC Space P/N	Q1 HEMT	$t_{d(ON)}$ (ns)	t_r (ns)	$t_{d(OFF)}$ (ns)	t_f (ns)
EPC7C002	FBG10N30	43.4	10.5	41.9	6.8

In all of the previous oscilloscope captures, the ON-delay time is defined as the time difference between the PWM input rising to the 50% point and the time it takes for the Q1 drain voltage to fall to 90% of its peak value. The rise time is defined as the time difference between the time it takes the Q1 drain voltage to fall from 90% of the peak value to 10% of the peak value. The OFF-delay time is defined as the time difference between the PWM input falling to the 50% point and the time it takes for the Q1 drain voltage to rise to 10% of its peak value. Finally, the fall time is defined as the time difference between the time it takes the Q1 drain voltage to rise from 10% of the peak value to 90% of the peak value.



NOTES:
1.) Resistors RT and RPU are EIA size 0805.
2.) Resistors RL1, RL2, RL3 and RL4 are EIA size 2512. Recommend Vishay CRCW-HP or equiv. pulse proof, high pulse handling type.
3.) Capacitors CB1 and CB2 are EIA size 0805.
4.) Capacitors CB3, CB4, CB5, CB6, CB7, CB8 and CB9 are EIA size 1210.
5.) TP1, TP2 and TP5 +/- are 0.040" dia. plated-through holes spaced 0.100" apart.
6.) TP3 and TP4 +/- are 0.040" dia. plated-through holes spaced 0.150" apart.
7.) Resistors RH1 and RH2 are EIA Size 2512 AC ground PCB etch conductivity "helpers".
8.) Resistor RG is EIA size 0603.

Figure 7. FBS-GAM01P-C-PSE and FSMD-B Demo Board Schematic Diagram.

FBS-GAM01P-C-PSE and FSMD-B Demo Board BOM

Table 4. EPC7C002 (100 V) BOM

Item	Qty	Ref. Des.	Description/Value	Manufacturer	Manufacturer P/N
1	1	CB1	0.1 µF/25 V/X7R/10%/0805 Ceramic Capacitor	Kemet	C0805C104K3RACAUTO
2	1	CB2	1.0 µF/25 V/X7R/10%/0805 Ceramic Capacitor	Kemet	C0805C105K3RACAUTO
3	6	CB3,CB4,CB5, CB7,CB8,CB9	0.22 µF/200 V/X7R/10%/1210 Ceramic Capacitor	TDK	CGJ6M3X7R2D224K200AA
4	1	CB6	0.1 µF/200 V/X7R/10%/1210 Ceramic Capacitor	Kemet	C1210C104K1RACAUTO
5	1	JIN	SMA/Vertical/50 Ω/Brass-Gold/SMT	Johnson/Cinch	142-0701-201
6	4	J1,J2,J3,J4	Through Hole Banana Jacks	Keystone	575-8
7	1	Q1	100 V/30 A HEMT FSMD-B Package	EPC SPACE	FBG10N30BX
8	1	RG	0R0/1%/0805 Thick Film Chip Resistor (Zero Ω Jumper)	Vishay	CRCW06030000Z0EA
9	2	RH1,RH1	0L300/1%/2512 Low Value Metal Strip SMT Resistor	Vishay	WSLF2512L3000FEA
10	1	RT	49R9/1%/0805 Thick Film Chip Resistor	Panasonic	ERJ-P06F49R9V
11	1	RPU	4.70 K/1%/0402 Thick Film Chip Resistor	Vishay	CRCW08054K70FKEAC
12	4	RL1,RL2,RL3,RL4	13R0 Ω/1%/2512 High Power Thick Filk Chip Resistor	Vishay	CRCW251213R0FKEGHP
13	1	U1	GAM01 Gate Driver	EPC SPACE	FBS-GAM01P-C-PSE
14	1	N/A	FBS GAM01-PSE/FSMD-B Evaluation PCB		47-042

Demo Board Modifications and “Cut In’s”

It is encouraged that end-users modify the load resistors and bypass capacitors to suit their application operating parameters. Other loads, such as inductors and transformers may be “cut into” the PCB in order to allow the GaN-driving-GaN GAM01P-C-PSE and FSMD-B gate driver and power HEMT tandem be used to obtain operating performance in the end-user’s actual application.

Printed Circuit Board and Layout Details

The printed circuit board (PCB) for the EPC7C002 Evaluation Board is constructed with four layers. The PCB is 4.95” x 3.95” and is 0.063” thick. The outer layers are 2 oz/in^2 and the inner layers are 1 oz/in^2 copper etch. All electronic components are SMT-packages and all connectors are through-hole.

The individual Gerber layers for the PCB are shown in Figures 8 through 16.

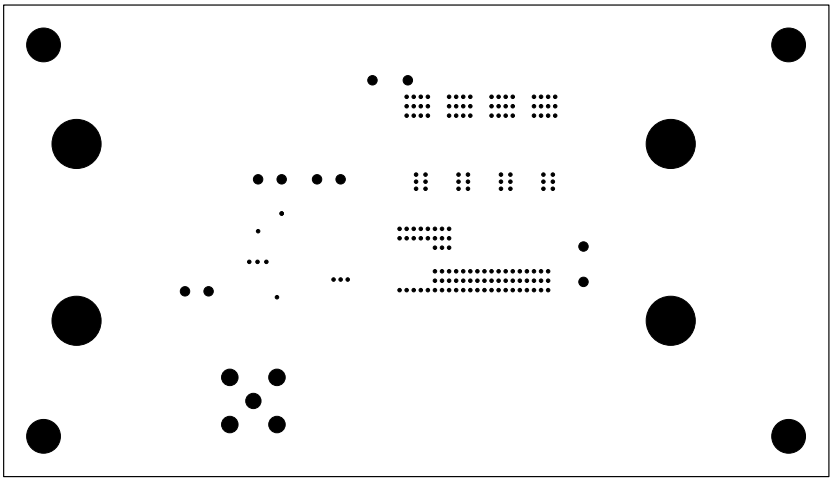


Figure 8. Excellon Drill File

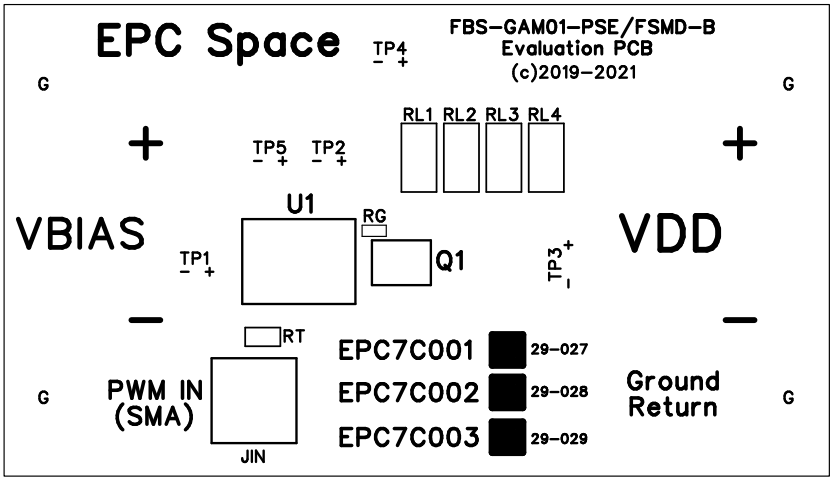


Figure 9. Top Side Silkscreen

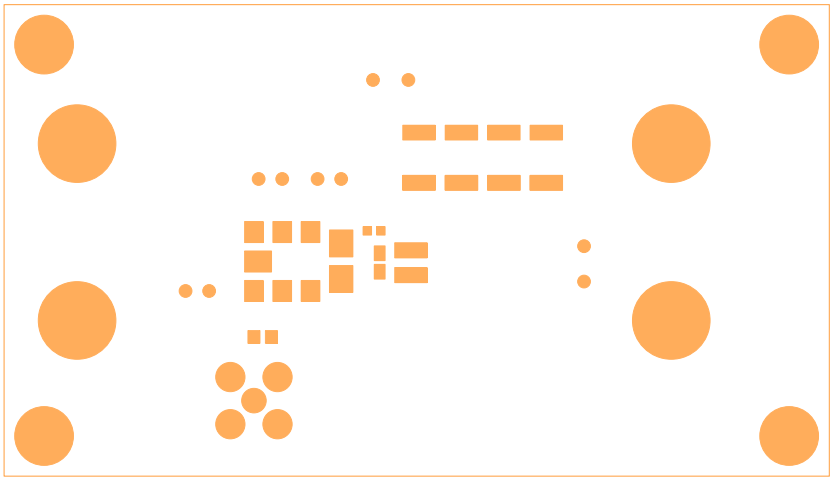


Figure 10. Top Side Solder Mask

Figure 11. Top Layer Copper (2 oz/in^2)

Figure 12. Inner Layer 1 Copper (1 oz/in^2)

Figure 13. Inner Layer 2 Copper (1 oz/in^2)

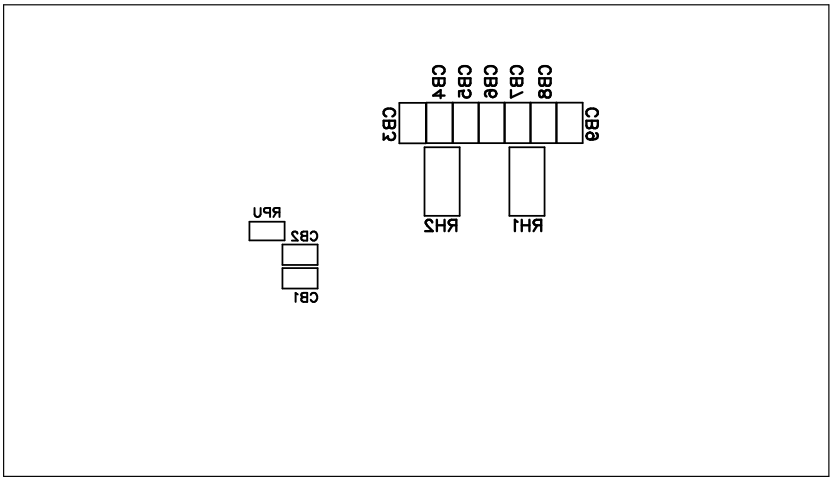


Figure 14. Bottom Side Silkscreen

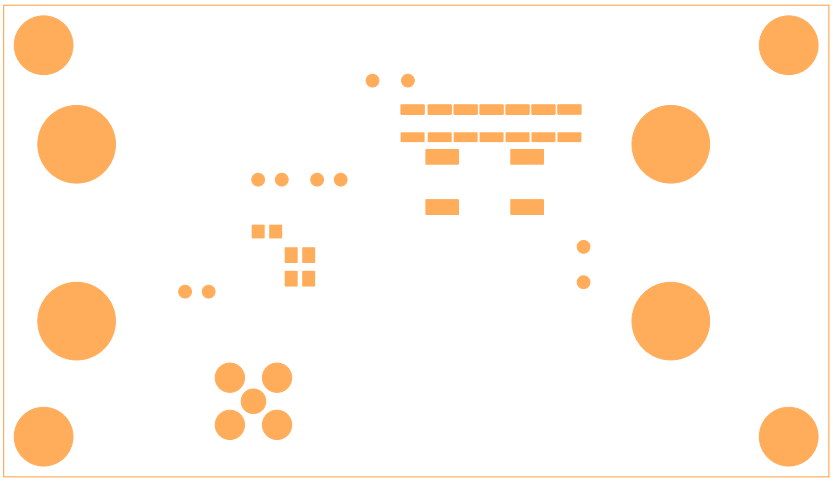


Figure 15. Bottom Side Solder Mask

Figure 16. Bottom Layer Copper (2 oz/in^2)

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Revisions

Revision	Date	Status
PR	3/6/2021	Pre-Release
--		Release
A		Revision A

Information subject to change without notice.
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Contact EPC Space for further information and to order:

Email: sales@epc.space

Phone: +1 978 208 1334

Website: epc.space

Address: 17 Parkridge Road
Unit # E
Haverhill, MA 01835
USA