ATTENTION
ELECTROSTATIC
SENSITIVE DEVICE

Proper ESD precautions should be employed when handling the EPC7C005 evaluation board to prevent damage to the components installed on the board.

Introduction

This document describes functionality, options and the recommended connection of the EPC7C005 FBS-GAM02 POL Evaluation Board to power supplies, electronic loads and monitoring instruments for proper operation for the evaluation of the switching operation and conversion efficiency performance of the EPC Space FBS-GAM02 Modules connected as a half-bridge POL power output stage.

This document also provides typical switching performance, typical efficiency performance, the schematic of the evaluation board, the bill of materials (BOM) and the PCB layout of the board in the form of layer-by-layer Gerber rendering of the evaluation printed circuit board.

Please consult the FBS-GAM02-P-C50 or FBS-GAM02-P-R50 for further details regarding the operation of the GAM02 Module.

Evaluation PCB Photograph

Figure 1a shows the top view and Figure 1b shows the bottom view of the EPC7C005 Evaluation Board. These pictures illustrate the component placements, power, load and input signal connections and the numerous test points available for monitoring by the end-user.

Description of Test Points

The description of each test point on the EPC7C001/2/3 demo board is found in Table 1.

Each set of test points (signal to be measured as indicated by "+", and ground as indicated by "-") have the physical spacings shown in Table 1 so as to facilitate easy oscilloscope probing by the end-user.

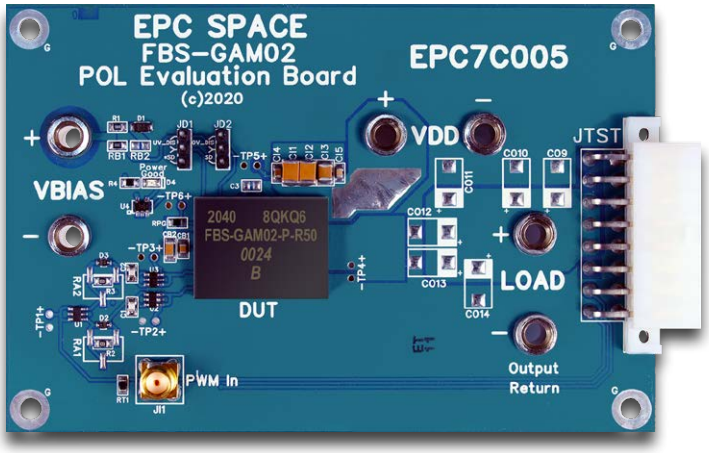


Figure 1a. EPC7C005 Evaluation Board (Top View)

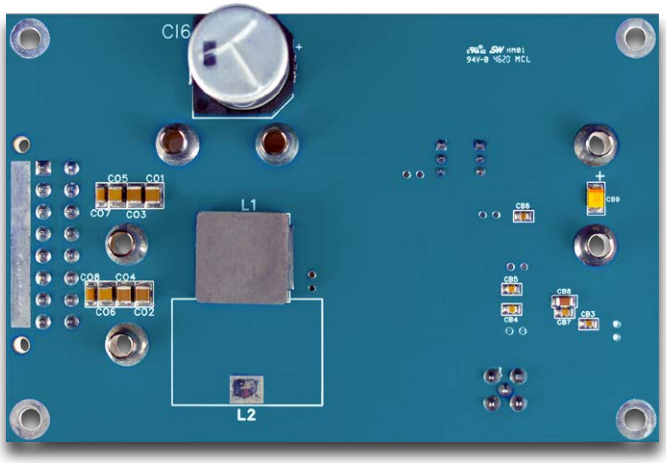


Figure 1b. EPC7C005 Evaluation Board (Bottom View)

Table 1. EPC7C005 Evaluation Board Test Point Identification

Test Point	+/- Spacing (in.)	Parametric Measurement Location
TP1	0.100	PWM Input Signal Monitor
TP2	0.100	BIN Logic Signal Monitor
TP3	0.100	TIN Logic Signal Monitor
TP4	0.100	Switching Node Signal Monitor
TP5	0.100	V_{DD} Monitor
TP6	0.100	PG (Power Good) Monitor

IMPORTANT NOTE: The "–" side of each test point is connected to the ground potential (i.e. 0 V_{DC}) of the Demo Board. ALWAYS make sure that the ground connection to the oscilloscope is connected to this point when power is applied to the board as damage may occur to the oscilloscope, the demo board or BOTH.

V_{LOAD} AC Signal Monitoring

Because the EPC7C005 Evaluation Board is configured as an "open loop" POL power stage, there is no test point provision for monitoring the AC signal at the output voltage V_{LOAD}. If it is desired to monitor the ripple voltage at V_{LOAD}, then a dual banana jack-to-BNC adapter, Pomona P/N 1269 "BNC (F) To Double Stacking Banana Plug" may be used as the "LOAD" banana jacks are 0.75" similarly-spaced.

Description of Connectors

There are four (4) connectors provided on the EPC7C005 Evaluation Board. The description of the functionality of each connector is shown in Table 2.

Table 2. EPC7C005 Evaluation Board Connector Description and Functionality

Connector	Description/Functionality
JI1	0-5 V PWM Input Signal
JD1	Pin 1-3 Open – DUT Normal Operation Pins 1-2 Shorted – UVLO Disabled Pins 2-3 Shorted – DUT Shut Down
JD2	Pin 1-3 Open – DUT Normal Operation Pins 1-2 Shorted – OVLO Disabled Pins 2-3 Shorted – DUT Shut Down
JTST	Remote power, load and measurement connector

JI1 "PWM In" Connector Detail

Connector JI1 is a standard SMA-style threaded connector.

JD1 and JD1 Connector Detail

Connectors are 0.100" center Molex C-Grid III-style pin connectors. It is recommended that if the disable or shutdown features of the evaluation board are utilized that a Samtec P/N SNT-100-BK-G-H 0.100" shunt/jumper w/handle be used to facilitate easy inclusion and removal from the board.

JTST Connector Detail

Connector JTST is provided such that efficiency measurements may be more easily and conveniently made by the end-user of the EPC7C005 Evaluation Board using automated power supplied, loads and PWM drive signals to obtain efficiency performance curves. The pinout for this connector is shown in Figure 2, looking into the pins, and the functionality of each pin is described in Table 3.

Figure 2. JTST Pinout

JTST Part Identity

Connector JTST is a 16 pin Molex Minifit Jr. style socket connector, Molex P/N 39-29-5163. There are several mating plugs including Molex P/N 39-01-2165, in the 5557 series.

Contacts for this connector are the Molex P/N 39-00-0080 for high current connections and the Molex P/N 39-00-0210 for low current connections. Both the contacts are in the Molex 5556 series.

Table 3. Demo Board EPC Space P/N vs. Q1 Identity vs. Load Resistance vs. Drain Current

JTST Pin #	Description/Functionality	JTST Pin #	Description/Functionality
1	V_{DD} Return	9	V_{DD}
2	V_{DD} Measurement Return	10	V_{DD} Measurement (Kelvin at DUT Pin 11)
3	Load Return	11	LOAD
4	Load Return	12	LOAD
5	Load Measurement Return	13	LOAD (V_{OUT}) Measurement
6	V_{BIAS} Return	14	VBIAS
7	DUT PG Return	15	DUT PG
8	PWM Return	16	PWM In (50 Ω)

"Power Good" LED, D4

The evaluation board is provided with a visual indication that V_{BIAS} power in the proper range for operation has been provided to the FBS-GAM02 DUT. Indicator LED D4 glows GREEN when V_{BIAS} power is applied.

IMPORTANT NOTE: If the "Power Good" LED is not illuminated, then there is either a problem with the VBIAS connection to the PCB, the on-card drive circuitry or the DUT has been damaged. DO NOT apply V_{DD} to the evaluation board in either case. Test point TP6 may be monitored to observe the state of the PG output on the FBS-GAM02 DUT. The voltage at this test point should be logic HIGH ("1"), at a voltage level greater than 4.5V if V_{BIAS} is set to 5 V, if the GAM02 is functioning properly. If the GAM02 is functioning properly, the LED and drive components (D4, R4 and U4) should be checked for proper operation and replaced if necessary.

Recommended Test Equipment Connections: AC Switching Operation

Figure 3 shows the recommended connection to/from the Evaluation Board for switching operation.

It is recommended that the connections to the EPC7C005 Evaluation Board from the V_{BIAS} (5.00 V) and V_{DD} power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable.

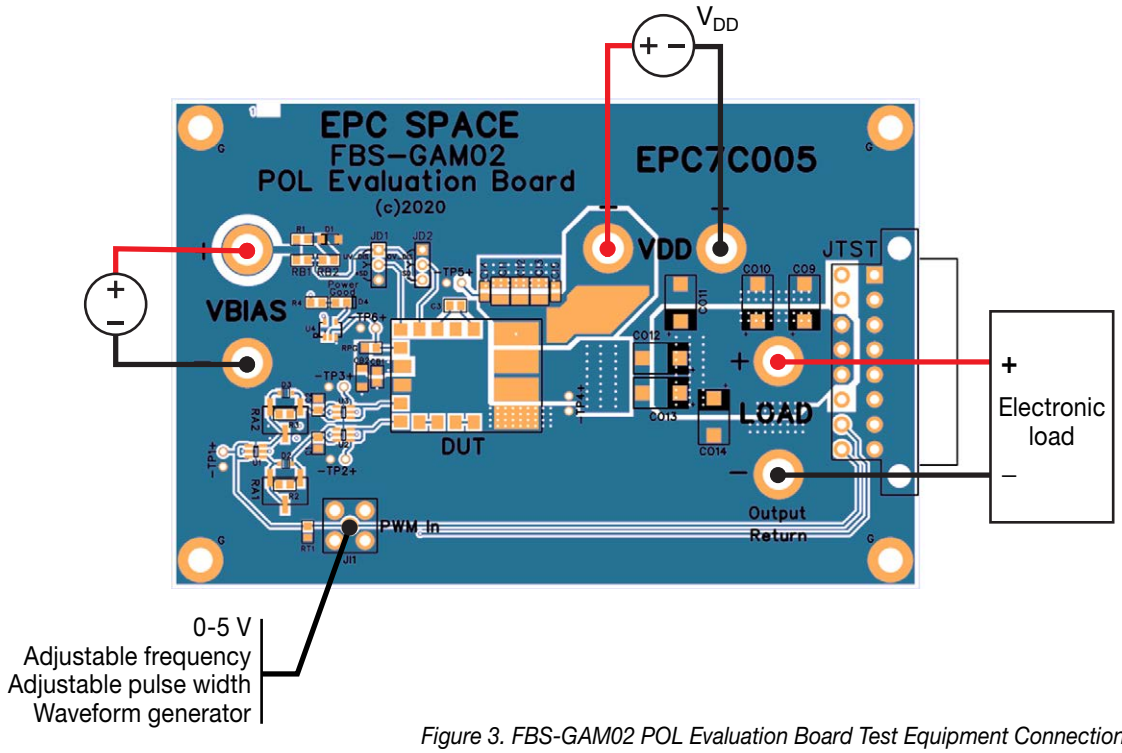


Figure 3. FBS-GAM02 POL Evaluation Board Test Equipment Connections: AC Switching Operation

Recommended Test Equipment: AC Switching Operation

The following test equipment is recommended to properly evaluate the EPC7C005 Evaluation Board as shown in Figure 3:

- 0-50 V, 10 A adjustable DC power supply
- 0-10 V, 100 mA adjustable lab power supply set to 5.00 V_{DC}
- 50 V/12 A electronic load
- 0-1.5 MHz, 0-5 V, adjustable duty cycle signal generator
- 500 MHz two channel oscilloscope
- Two 10:1 passive oscilloscope probes configured with 0.100" spacing between probe tip and ground
- Quantity 6 – 12" to 18" banana plug-to-banana plug cables

Recommended Test Equipment Connections: Conversion Efficiency

Figure 4 shows the recommended connection to/from the Evaluation Board for switching operation.

It is recommended that the connections to the EPC7C005 Evaluation Board from the V_{BIAS} (5.00 V) and V_{DD} power supplies, and the electronic load, be made with banana plug-to-banana plug cables, as short as possible length and twisted to prevent noise pickup. The connection from the pulse/frequency generator to connector J1 should be made via an SMA (board)-to-BNC (generator) cable. Voltages V_{DD}, V_{BIAS} and V_{LOAD} should be monitored/measured at the associated banana jacks on the board.

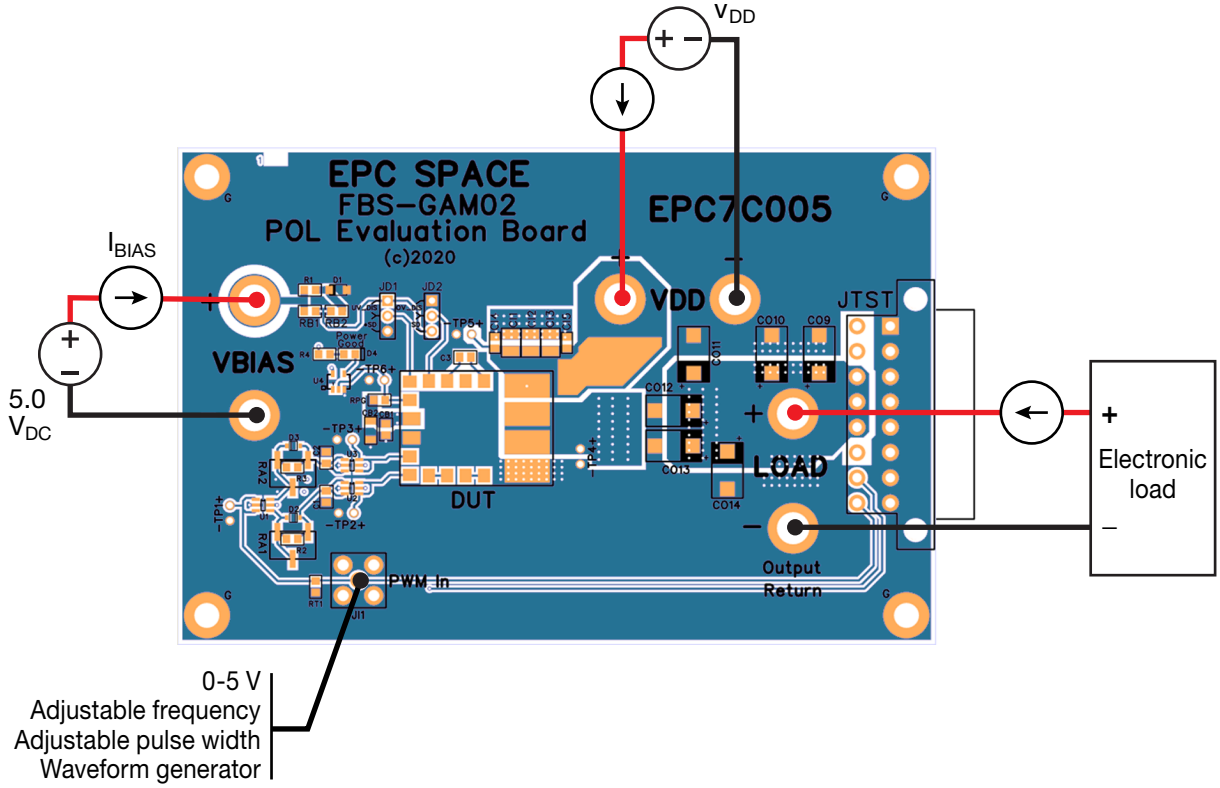


Figure 4. FBS-GAM02 POL Evaluation Board Test Equipment Connections: Conversion Efficiency

Recommended Test Equipment: Conversion Efficiency

The following test equipment is recommended to properly evaluate the EPC7C005 Evaluation Board as shown in Figure 4:

- 0-50 V, 10 A adjustable DC power supply
- 0-10 V, 100 mA adjustable lab power supply set to 5.00 V_{DC}
- 50 V/12 A electronic load
- 0-1.5 MHz, 0-5 V, adjustable duty cycle signal generator
- 500 MHz two channel oscilloscope
- Two 10:1 passive oscilloscope probes configured with 0.100" spacing between probe tip and ground
- Quantity 3 – Precision digital voltmeters (one to monitor V_{DD}, VBIAS and the load voltage, V_{LOAD});
- Quantity 3 – Precision digital ammeters (one to monitor I_{DD}, I_{BIAS} and the load current, I_{LOAD});
- Quantity 15 – 12" to 18" banana plug-to-banana plug cables

EPCS EPC7C005 Evaluation Board Minimum and Maximum Ratings

The EPC7C005 is rated for the following operation:

- V_{DD}: 5 V_{DC} to 50 V_{DC}
- I_{LOAD}: 0 A minimum to 10 A maximum.
- V_{BIAS}: 6.0 V_{DC}, unclamped (RB1 present/RB2 NOPOP, default)
- 7.5 Vpeak/10 ms, clamped (RB1 NOPOP/RB2 present, customer option)
- PWM IN: 5 V maximum/200 kHz to 1.5 MHz/90% duty cycle maximum

BIN-TIN and TIN-BIN Logic Input Dead Times

The EPC7C005 Evaluation Board is shipped with a fixed, approximate 100 ns dead time between the BIN and TIN and TIN and BIN logic inputs being asserted to prevent the possibility of cross-conduction/shoot-through occurring during the evaluation board's operation. To improve high-frequency efficiency, the dead time may be decreased to 75 ns, minimum, by replacing the 100 pF capacitors in reference designations C1 and C1 with 75 pF values (75 pF, COG, 5%, 0805).

IMPORTANT NOTE: The dead time should NEVER be reduced below 75ns

Additionally, a trimpot option is provided on the evaluation board to allow the end-user to more easily adjust dead times to obtain the best value for the given end-use application. Fixed 1.00 KΩ resistors may be removed and be replaced with 1 KΩ multiturn trimpots in locations RA1 and RA2. The PCB footprints for these trimpots are for the Vishay P/N TS63Y102KT20 devices. The BIN-TIN and TIN-BIN dead times may be adjusted from 75 ns to 100 ns using these trimpots. Again, the dead time should **NEVER** be reduced below 75 ns.

IMPORTANT NOTE: It is recommended that prior to the application of V_{DD} for testing the evaluation board that the BIN-TIN and TIN-BIN dead times are verified by applying V_{BIAS} to the circuit and monitoring TP2 and TP3 to ensure that the resultant dead times are either 100 ns (default as shipped) or the desired value set by the end-user.

AC Switching Operation Test Procedure

With the evaluation board connected to the test equipment as shown in Figure 3, the switching node (SN) waveform may be monitored using the following test sequence:

1. Insert a 0.100" spaced probe/ground into test point TP4, observing the proper polarity for ground
2. Apply the desired PWM signal
3. Turn on V_{BIAS}
4. Adjust the electronic load to the desired output current value and enable the output
5. Turn on V_{DD}

When the POL evaluation circuit is ON and running, the load current (I_{LOAD}) and the PWM duty cycle may be adjusted to obtain the desired value of V_{LOAD}/V_{OUT}.

The resultant SN waveform may be captured for review/analysis.

IMPORTANT NOTE: NEVER adjust the PWM frequency while the EPC7C005 POL circuit is ON and running. Damage/destruction of the FBS GAM02 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks or connector JTST on the evaluation board.

Conversion Efficiency Test Procedure

With the evaluation board connected to the test equipment as shown in Figure 4, the switching node (SN) waveform may be monitored using the following test sequence:

1. Apply the desired PWM signal
2. Turn on V_{BIAS}
3. Adjust the electronic load to the desired output current value and enable the output
4. Turn on V_{DD}

When the POL evaluation circuit is ON and running, the load current (I_{LOAD}) and the PWM duty cycle may be adjusted to obtain the desired value of V_{LOAD}/V_{OUT} at each operating point. A most accurate efficiency is obtained if V_{DD} is adjusted to the same value at each value of load current and then the PWM duty cycle is subsequently adjusted to desired value of V_{LOAD}/V_{OUT}.

The conversion efficiency (η) at each operating point is defined as:

$$\eta = (V_{LOAD} \cdot I_{LOAD}) / [(V_{DD} \cdot I_{DD}) + (V_{BIAS} \cdot I_{BIAS})]$$

IMPORTANT NOTE: NEVER adjust the PWM frequency while the EPC7C005 POL circuit is ON and running. Damage/destruction of the FBS GAM02 DUT device may result.

The previous procedure and test sequence are applicable regardless if the power, load and PWM signals are applied via the banana jacks or connector JTST on the evaluation board.

BIN-TIN and TIN-BIN Dead Time Typical Waveforms

The waveform shown in Figure 5 is typical of the BIN-TIN and TIN BIN dead times for C1 = C2 = 75 pF. Logic input BIN is the yellow trace and TIN is blue:

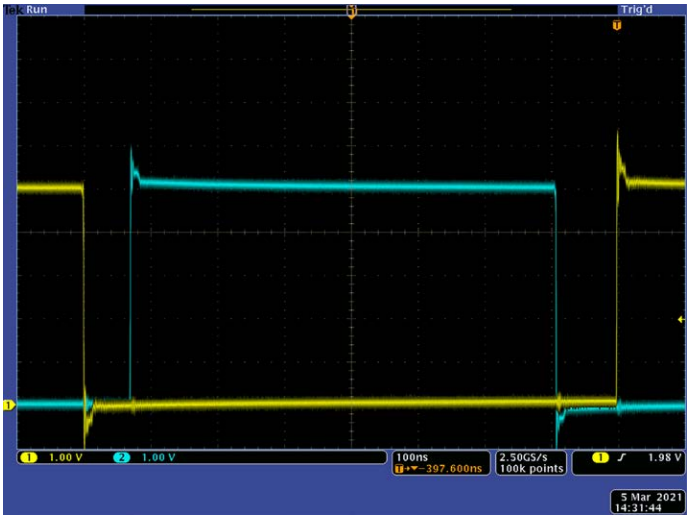


Figure 5. FBS-GAM02 POL Evaluation Board BIN-TIN and TIN BIN Logic Input Dead Time

Typical Switching Node (SN) Waveform

The waveform shown in Figure 6 is typical of the switching node for Evaluation Board operation at V_{DD} = 25 V, V_{LOAD} = 5.0 V, switching frequency = 200 kHz and I_{LOAD} = 10 A:

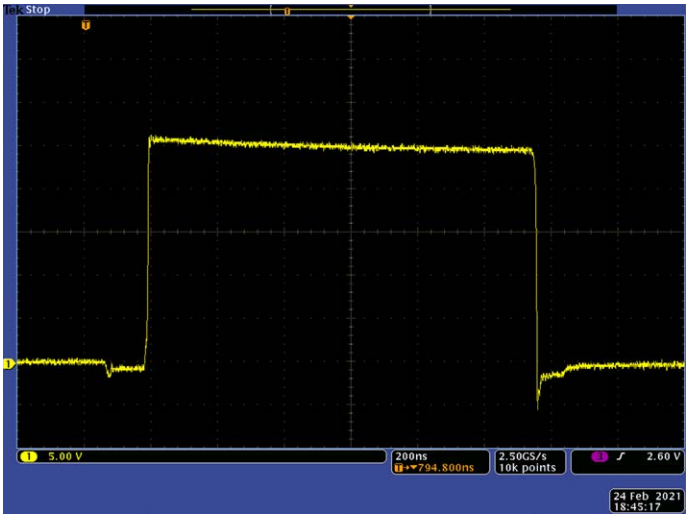


Figure 6. FBS-GAM02 POL Evaluation Board Typical Switching Node Waveform

The waveform shown in Figure 7 is typical of the switching node rise time for Evaluation Board operation at the same conditions as in Figure 6:

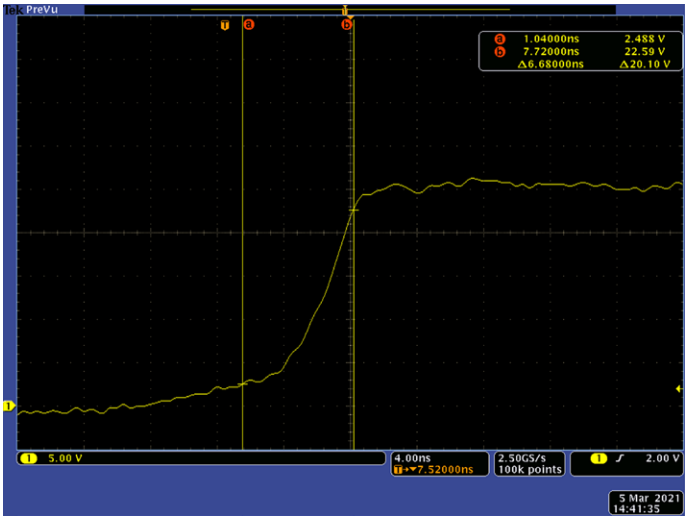


Figure 7. FBS-GAM02 POL Evaluation Board Typical Rise Time Waveform

The waveform shown in Figure 8 is typical of the switching node fall time for Evaluation Board operation at the same conditions as in Figure 6:

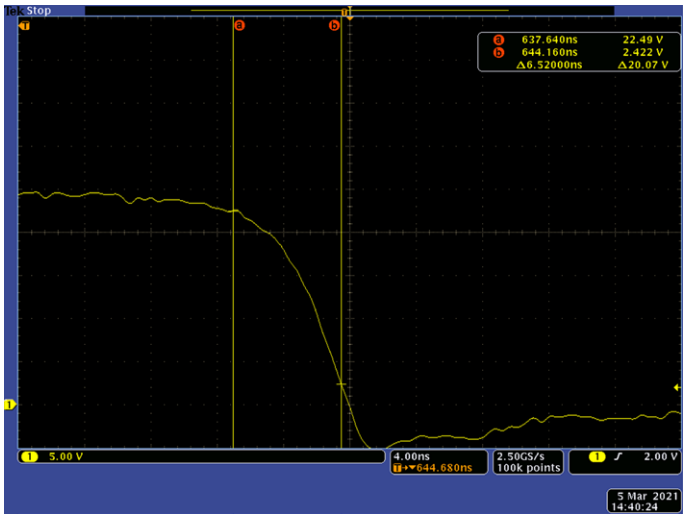


Figure 8. FBS-GAM02 POL Evaluation Board Typical Fall Time Waveform

Typical Conversion Efficiency Graphs

The graph shown in Figure 9 is typical of the EPC7C005 evaluation board conversion efficiency with respect to switching frequency for the conditions listed on the graph.

The graph shown in Figure 10 is typical of the EPC7C005 evaluation board conversion efficiency with respect to dead time for the conditions listed on the graph.

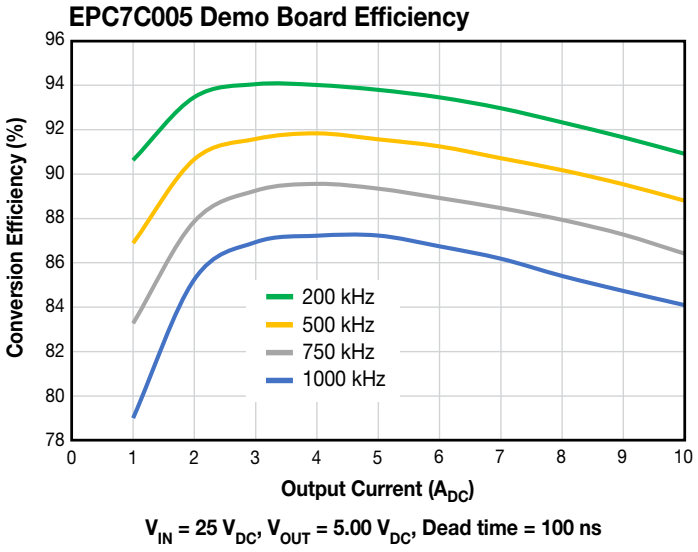


Figure 9. FBS-GAM02 POL Evaluation Board Typical Conversion Efficiency

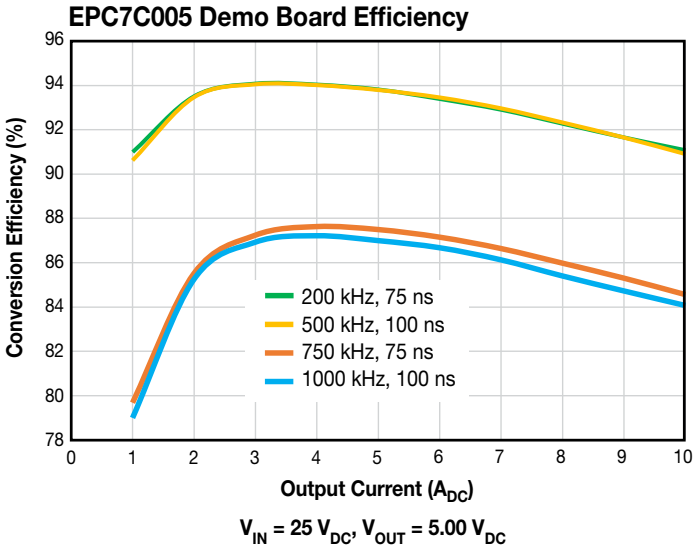


Figure 10. FBS-GAM02 POL Evaluation Board Typical Conversion Efficiency

Optimization of Conversion Efficiency Performance

No attempt has been made to optimize the conversion efficiency performance of the EPC7C005 FBS-GAM02 POL evaluation board. The board was, however, optimized for switching performance and to provide the best switching waveforms in terms of minimizing stray inductances in the power loop to prevent transient overshoots at the switching node and V_{DD}.

Because the evaluation board was intended to be used over a wide range of input and output voltages, load currents and switching frequencies, there could be no "optimized" set of components used for all possible applications to achieve the highest possible conversion efficiency. As such, optimization of the evaluation board for a particular customer end-use application is left to the designer who is evaluating this board. To this end, the output inductor L1 may be changed for a different value in the same package style. The inductor utilized on the evaluation board is in the Vishay IHLP6767 series, so other inductance values (with lower DC resistances and AC core losses) may be chosen for the particular switching frequency desired. In addition to L1, an unpopulated output inductor L2 is also included in the evaluation board layout. If the smallest size/area/volume isn't the primary consideration in the design, if L1 is depopulated, L2 may be used as the output inductor. It has larger physical size, but has lower DC resistance, lower AC core losses and higher saturation current characteristics. Inductor L2 is in the Bourns PQ2614BLA series. The use of L2 allows for increases in conversion efficiency by over 2%, but at a physical size penalty.

In order to improve performance, other capacitance values and rated voltages may be substituted for the V_{DD} bulk filter capacitor CI6. The capacitor utilized on the evaluation board is in the Panasonic K16 size form factor. The as-shipped rated voltage is 80V to provide adequate de-rating when the evaluation board is operated with a V_{DD} of 50V, but if lower operating voltages are required, the capacitance value of CI6 may be increased substantially. Additionally, because of the pad sizes of the PCB shape for this capacitor, other smaller case styles may be "cut in" to replace the as-shipped component.

In order to reduce the amount of AC ripple at the LOAD output, there are unpopulated tantalum capacitor shape placeholders whose reference designations are CO9-CO14. The footprints provided are intended for a "D" case tantalum capacitor. If tantalum capacitors are undesirable, the footprints for CO9-CO14 can accept 1812 to 2020-sized ceramic capacitor body sizes.

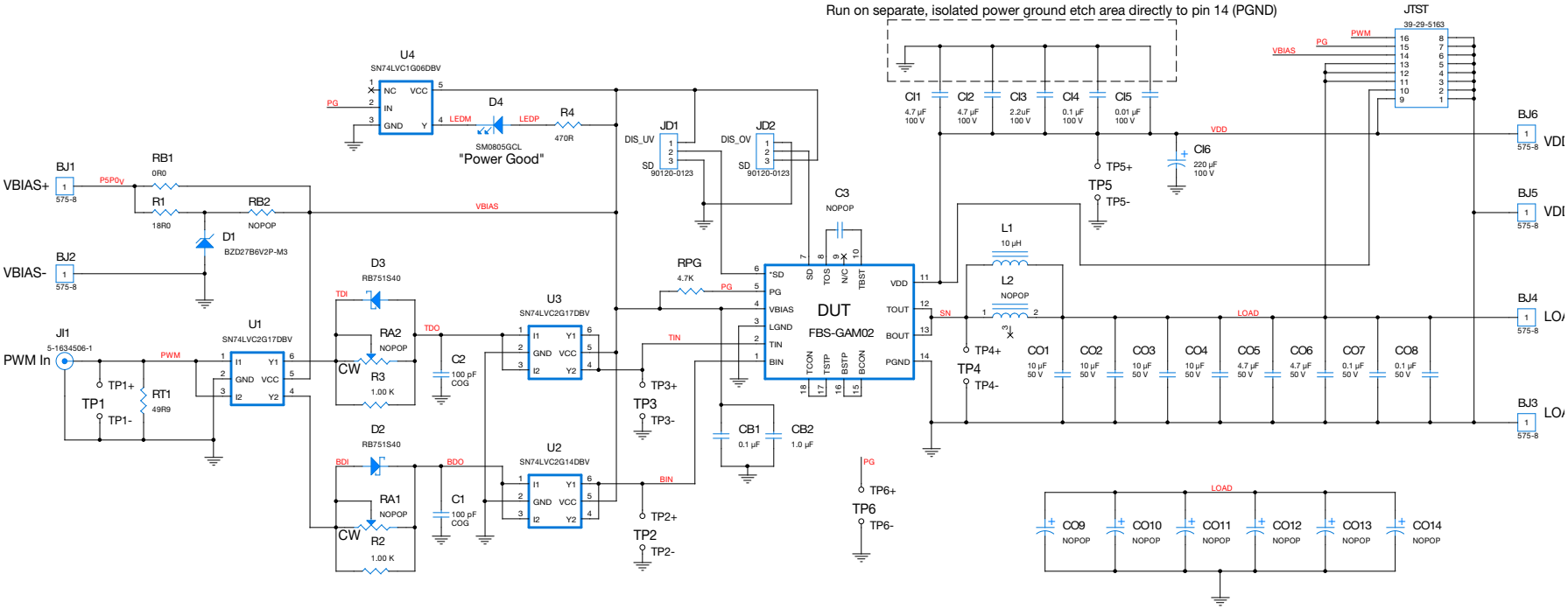
High-Side Bootstrap Capacitor C3

A non-populated component shape, C3, has been provided just adjacent to the DUT for additional high-side driver bootstrap capacitance for operation of the evaluation board at frequencies lower than 200kHz. A capacitance of 0.15 µF is recommended is switching frequencies below 200kHz are employed. The capacitor is 0805 size and should be rated for 25 V_{DC}.

V_{BIAS} Voltage Clamp

An option is provided on the evaluation board to provide voltage clamping of the VBIAS supply to a level of ~6.2 V_{DC} if transients are expected on this power supply in the end circuit application. The evaluation board is shipped with this function disabled. However, the designer may enable this feature by removing the zero Ω jumper resistor in designation RB1, leaving RB1 NOPOP, and place it in RB2.

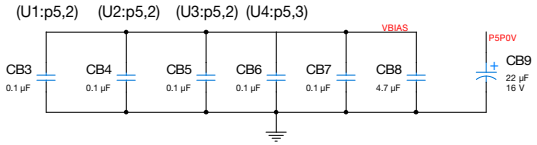
IMPORTANT NOTE: At NO TIME should both designation RB1 and RB2 be populated.



Optional Output Filter Capacitors (Tantalum D-Case, EIA 7434)

NOTES:

1.) All capacitors are X7R and 50V, unless otherwise specified.
2.) Place bypass capacitors directly beneath associated IC's.
3.) End-user may omit resistors R2 and R3 and populate potentiometers RA1 and RA2 (Vishay TS63Y type) to adjust dead time.
4.) All resistors are 0805-size unless otherwise specified.
5.) Resistors RB1 and RB2 select if direct VBIAS or clamped VBIAS protection is provided for the DUT. RB1 provides direct, and is populated. RB2 provides the clamped protection, and is NOPOP.
6.) Inductor L1 is a Vishay IHLP 6767 size, and is populated. Inductor L2 is a Bourns PQ2614BLA size, and is NOPOP.
7.) Connector JTST is provided to accurately measure conversion efficiency at various operating conditions.



VBIAS Power Suppy Bypass Capacitors

Figure 11. EPC7C005/FBS-GAM02 POL Evaluation Board Schematic Diagram

EPC7C005 / FBS-GAM02-P-R50 POL Evaluation Board BOM

The BOMs for the FBS-GAM02-P-C50 POL Evaluation Board is shown in Table 4.

Table 4. EPC7C005/FBS-GAM02-P-C50 POL Evaluation Board Bill of Materials

Item	Qty	Ref. Des.	Description/Value	Manufacturer	Manufacturer P/N	Size/ Package
1	1	DUT	GaN Driver Module	EPC Space	GAM02-P-C50	19 mm x 9.7mm
2	6	BJ1, BJ2, BJ3, BJ4, BJ5, BJ6	Solderable Banana Staking Jack	Keyston+ F18:H40e	575-8	0.208" Dia. Hole
3	6	CB1, CB3, CB4, CB5, CB6, CB7	0.1 µF/25 V/X7R/10%/AEC-Q200/0805 Ceramic Capacitor	Kemet	C0805C104K3RACAUTO	C0805
4	1	CI4	0.1 µF/100 V/X7R/10%/AEC-Q200/0805 Ceramic Capacitor	Kemet	C0805C104K1RECAUTO	C0805
5	2	CO7,CO8	0.1 µF/50 V/X7R/10%/AEC-Q200/1206 Ceramic Capacitor	Kemet	C1206F104K5RACAUTO	C1206
6	1	CB2	1.0 µF/25 V/X7R/10%/1206 Ceramic Capacitor	Kemet	C1206C105K3RACAUTO	C1206
7	1	CB8	4.7 µF/25 V/X7R/10%/AEC-Q101/1206 Ceramic Capacitor	AVX	12063C475K4T2A	C1206
8	2	CO5, CO6	4.7 µF/50 V/X7R/10%/1210 Ceramic Capacitor	Kemet	C1210C475K5RACAUTO7210	C1210
9	2	CI1,CI2	4.7 µF/100 V/X7R/10%/1210 Ceramic Capacitor	Kemet	C1812C225K1RACAUTO	C1812
10	2	CI6	220 µF/100 V/20%/FK Series/V Type/K16 Size Aluminum Electrolytic Capacitor	Panasonic	EEVFK2A221M	Panasonic K16
11	1	CB9	22 µF/16 V/Tantalum/10%/B Case SMT Capacitor	AVX	TRJB226K016RRJ	TANT_B
12	6	CI3	2.2 µF/100 V/X7R/10%/AEC-Q200/1210 Ceramic Capacitor	Kemet	C1210C225K1RACAUTO	C1210
13	4	CO1, CO2, CO3, CO4	10 µF/50 V/X7R/10%/0805 Ceramic Capacitor	Taiyo Yuden	UMK325AB7106KMHP	C1210
14	1	CI5	0.01 µF/100 V/X7R/10%/AEC-Q200/0805 Ceramic Capacitor	AVX	08051C103K4T2A	C0805
15	NOPOP	C3	NOPOP			C0805
16	NOPOP	CO9, CO10, CO11, CO12, CO13, CO14	NOPOP			TANT_D
17	1	D1	6.2 V/2%/100 mA/SMF Zener Diode w/Surge Current Specification	Vishay	BZD27B6V2P-M3	SMF
18	2	D2,D3	0.12 A/40 V/SOD-323 Schottky Diode	Nexperia	RB751V40,115	SOD-323
19	1	D4	568 nm Green Water Clear/0805 Package LED	Bivar	SM0805GCL	D0805
20	2	JD1, JD2	3 Pin Straight Connector/Through-Hole/C-Grid III	Molex	90120-0123	0.1" Centers
21	2	SB1, SB2	0.100" Shunt/Shorting Bar w/Handle	Samtec	SNT-100-BK-G-H	N/A
22	1	JI1	SMA/Vertical/50 Ω/Brass-Gold/Through Hole	Amphenol	901-144-8RFX	901-144-8RFX
23	1	JTST	Mini-Fit Jr. Header, Dual Row, Right-Angle, w/Mounting Flange, 16 Pin/UL-94 V-2/Au	Molex	39-29-5163	39-29-5163
24	1	L1	20 A/10 µH Power Inductor/10.91 mΩ/0.67"x0.67"	Vishay/Dale	IHLP6767GZER100M5A	IHLP6767
25	NOPOP	L2	NOPOP	Bourns	PQ2614BLA Series	PQ2614BLA
26	NOPOP	RA1, RA2	1K Ω/Multi-turn/Vertical Adjustment/SMT Potentiometer	Vishay	TS63Y102KT20	TS63Y
27	1	RB1	0 Ω Jumper Resistor/0805	Vishay	CRCW08050000Z0EA	R0805
28	NOPOP	RB2	0 Ω Jumper Resistor/0805	Vishay	CRCW08050000Z0EA	R0805
29	1	RPG	4.70 K/1%/0805/Thick Film Chip Resistor	Vishay	CRCW08054K70FKEA	R0805
30	1	RT1	49R9/1%/0805/Thick Film Chip Resistor	Vishay	CRCW080549R9FKEA	R0805
31	1	R1	18R0/1%/0805 High Power Thick Film Chip Resistor	Vishay	CRCW080518R0FKEAHP	R0805
32	2	R2, R3	1.00 K/1%/0805 Thick Film Chip Resistor	Vishay	CRCW08051K00FKEA	R0805
33	1	R4	470R/1%/0805 Thick Film Chip Resistor	Vishay	CRCW0805470RFKEA	R0805
34	2	U1, U3	Dual Schmitt Trigger B µFfer/Little Logic/1.65-5.5 V/LVC/SOT-23-6	TI	SN74LVC2G17DBV	SOT-23-6
35	1	U2	Dual Schmitt Trigger Inverter/Little Logic/1.65-5.5 V/LVC/SOT-23-6	TI	SN74LVC2G14DBV	SOT-23-6
36	1	U4	Single Open-Drain Inverter/Little Logic/1.65-5.5 V/LVC/SOT-23-5	TI	SN74LVC1G06DBV	SOT-23-5
37	4	Misc. Hardware	Spacer/Hex/PVC/6-32/0.75" Length	Essentra	144-HS-6-6	N/A
38	4	Misc. Hardware	Screw/6-32/Nylon/Round head/Slotted/0.5" Length	Essentra	010632R050	N/A
39	1	PCB	4.95" x 3.25 x 0.063" 4 Layer FR-4 PCB, Double-Sided	TBD	47-TBD	N/A

Printed Circuit Board and Layout Details

The printed circuit board (PCB) for the EPC7C005 FBS-GAM02 POL Evaluation Board is constructed with four layers. The PCB is 4.95” x 3.95” and is 0.063” thick. The outer layers are 2 oz/in^2 and the inner layers are 1 oz/in^2 copper etch. All electronic components are SMT-packages and all connectors are through-hole. The PCB shape of connector JTST overhangs the board to facilitate ease of external connection.

The individual Gerber layers for the PCB are shown in Figures 12 to 20.

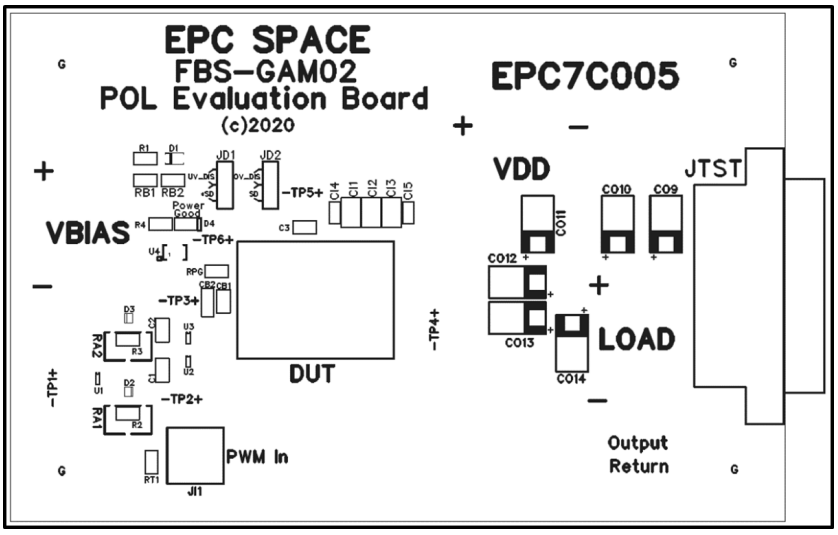


Figure 12. EPC7C005/FBS-GAM02 POL Evaluation Board Top Silkscreen

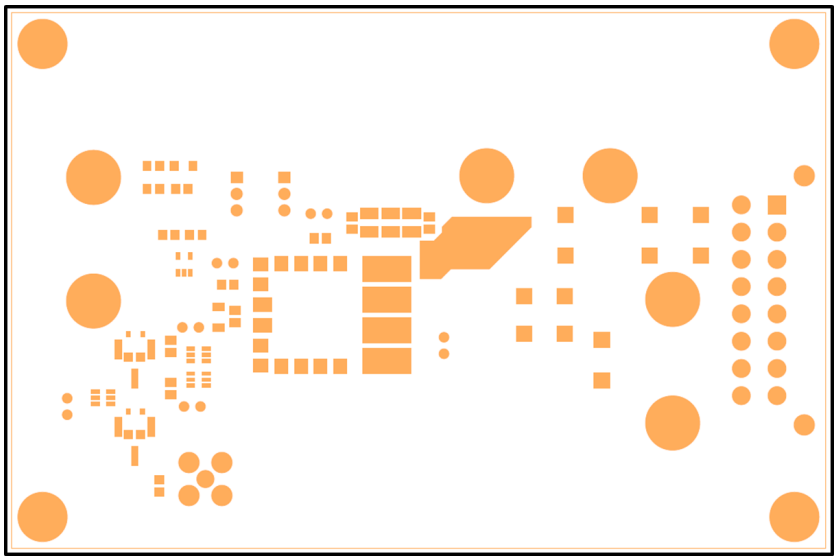


Figure 13. EPC7C005/FBS-GAM02 POL Evaluation Board Top Solder Mask

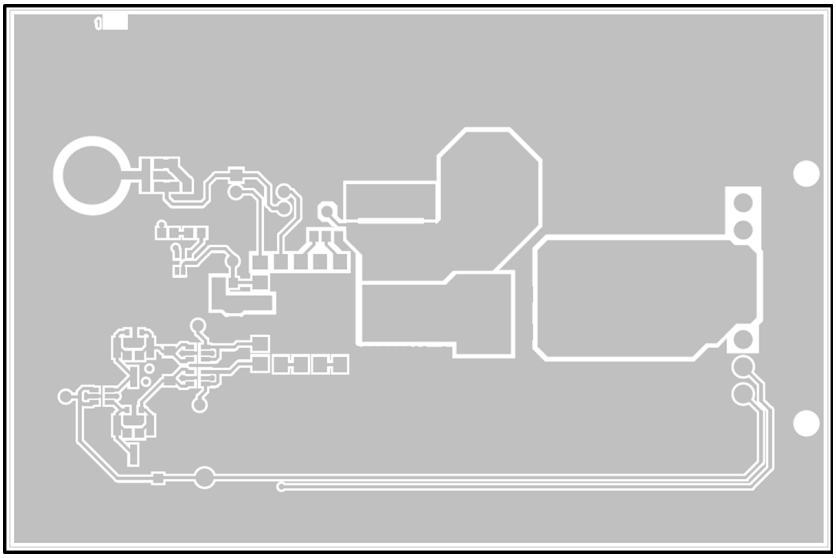


Figure 14. EPC7C005/FBS-GAM02 POL Evaluation Board Top Copper Etch (2 oz)

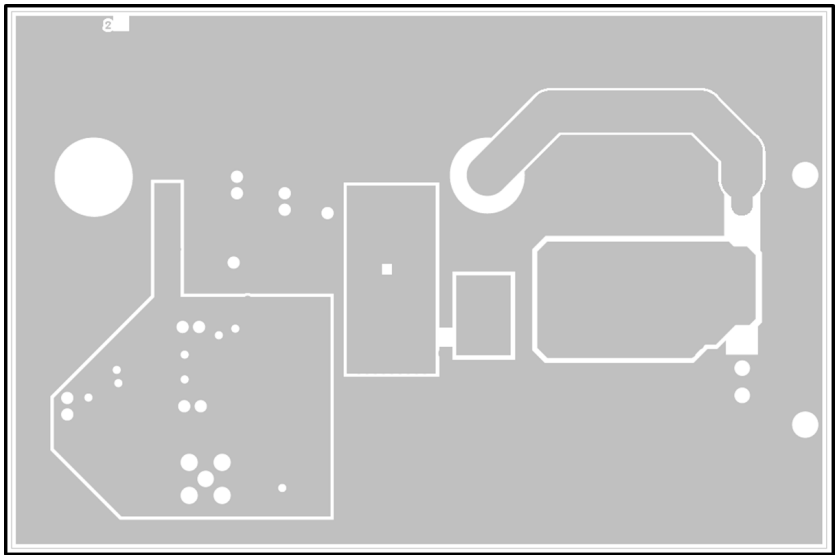


Figure 15. EPC7C005/FBS-GAM02 POL Evaluation Board Inner Layer 1 Copper Etch (1 oz)

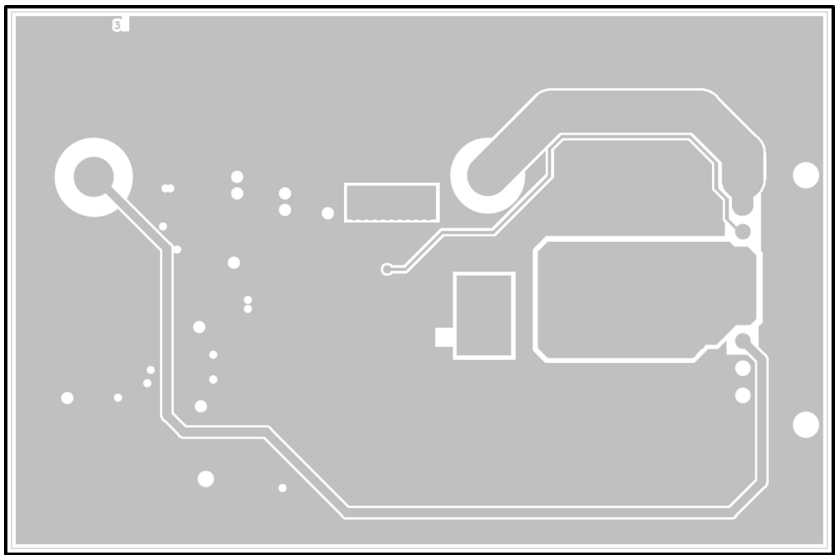


Figure 16. EPC7C005/FBS-GAM02 POL Evaluation Board Inner Layer 2 Copper Etch (1 oz).

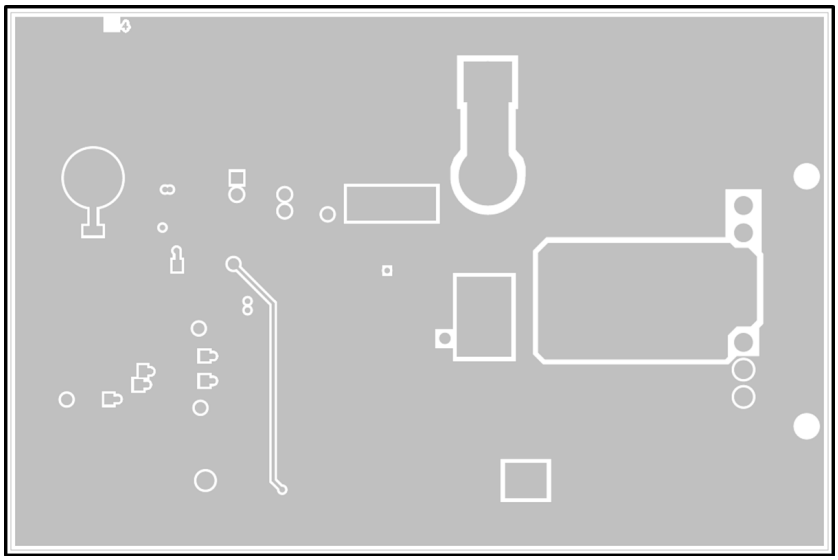


Figure 17. EPC7C005/FBS-GAM02 POL Evaluation Board Bottom Copper Etch (2 oz)

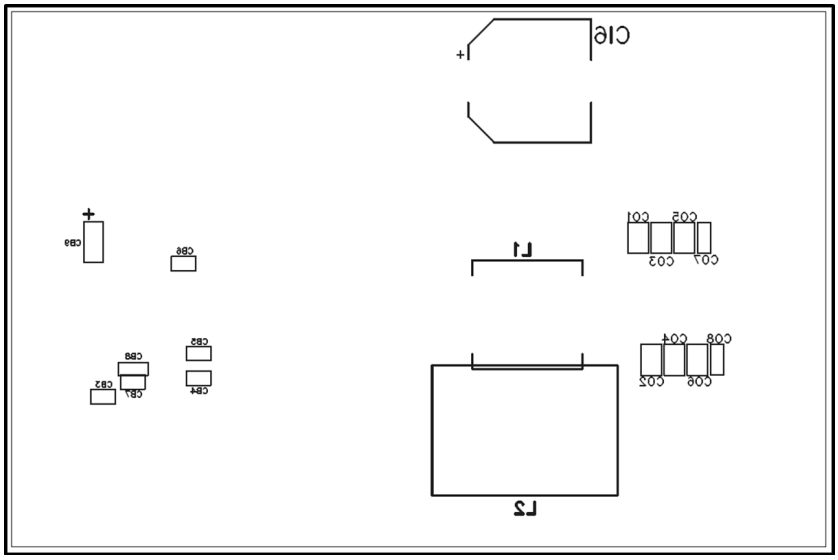


Figure 18. EPC7C005/FBS-GAM02 POL Evaluation Board Bottom Silkscreen

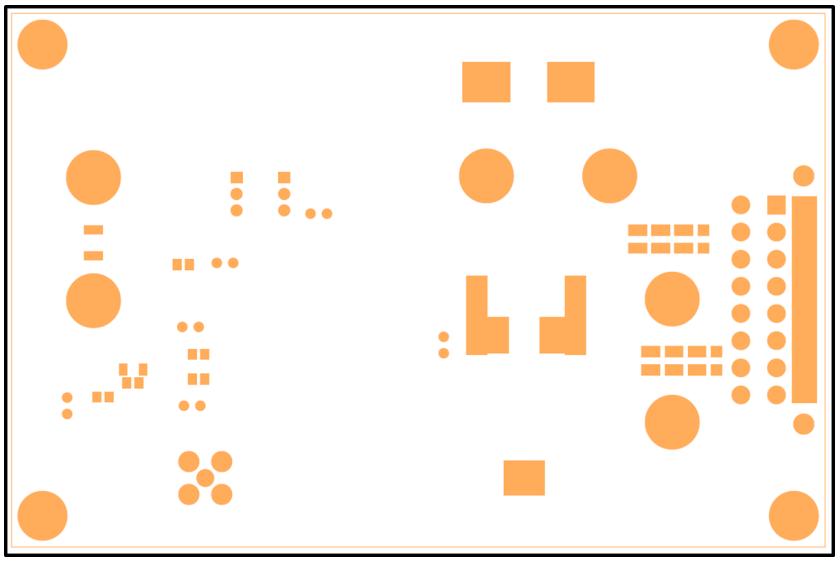


Figure 19. EPC7C005/FBS-GAM02 POL Evaluation Board Bottom Solder Mask

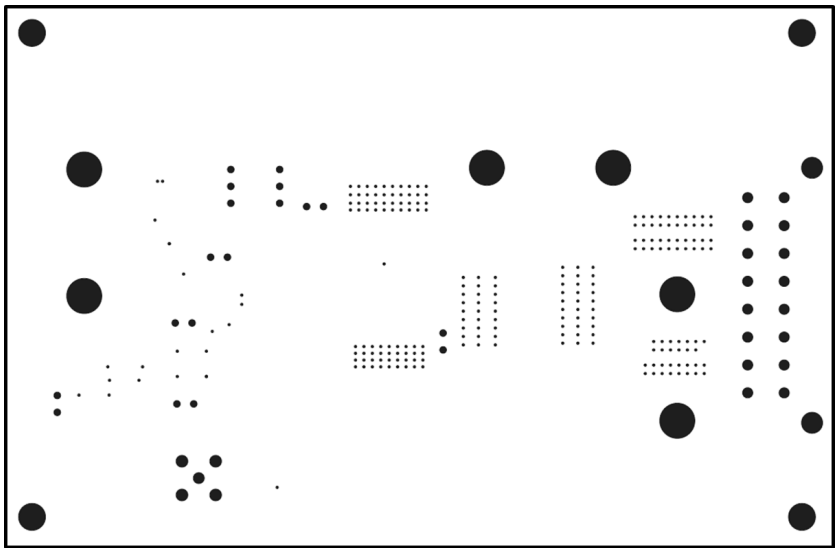


Figure 20. EPC7C005/FBS-GAM02 POL Evaluation Board Drill Pattern

Disclaimers

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE. EPC Space Corporation, its affiliates, agents, employees, and all persons acting on its or their behalf (collectively, "EPC Space"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product. EPC Space makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose. To the maximum extent permitted by applicable law, EPC Space disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability. Statements regarding the suitability of products for certain types of applications are based on EPC Space market knowledge of typical requirements that are often placed on similar technologies in generic applications. Product specifications do not expand or otherwise modify EPC Space terms and conditions of purchase, including but not limited to the warranty expressed therein. Except as expressly indicated in writing, EPC Space products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the EPC Space product could result in personal injury or death. Customers using EPC Space products not expressly indicated for use in such applications do so at their own risk. Please contact authorized EPC Space personnel to obtain written terms and conditions regarding products designed for such applications. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of EPC Space. Product names and markings noted herein may be trademarks of their respective owners.

Export Administration Regulations (EAR)

The products described in this datasheet could be subjected to the Export Administration Regulations (EAR). They may require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

International Traffic in Arms Regulations (ITAR)

The products described in this datasheet could be subjected to the International in Arms Regulations (ITAR). They require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Patents

EPC Space holds numerous U.S patent. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S Patent laws

eGaN® is a registered trademark of Efficient Power Conversion Corporation, Inc. Data and specification subject to change without notice.

Revisions

Revision	Date	Status
PR	3/6/2021	Pre-Release
--		Release
A		Revision A

Information subject to change without notice.
Revised July, 2021

Contact EPC Space for further information and to order:

Email: sales@epc.space

Phone: +1 978 208 1334

Website: epc.space

Address: 17 Parkridge Road
Unit # E
Haverhill, MA 01835
USA