

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, GALLIUM NITRIDE, HIGH ELECTRON MOBILITY TRANSISTOR (HEMT),
RADIATION HARDENED, ENHANCEMENT MODE,
TYPES 2N7678UFG, 2N7679UFD, 2N7680UFG, 2N7681UFG, QUALITY LEVELS JANTX, JANTXV, JANS, JANHC,
AND JANKC

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an enhancement-mode Gallium Nitride, radiation hardened (Total Dose and Single Event Effects (SEE)), High Electron Mobility Transistor (HEMT). Two levels of product assurance (JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#), and two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device type. Enhancement Mode Gallium Nitride devices are not sensitive to total ionizing dose and will be provided as level H for JANTX, JANTXV and JANS product assurance levels.

1.2 Package outlines. The device package for the encapsulated device types are as follows: (UFGC, and UFDC) in accordance with [figure 1](#). The dimensions and topography for JANHC and JANKC unencapsulated die is as follows: The A version die in accordance with [figure 2](#) and [figure 3](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T $T_C =$ $+25^\circ\text{C}$ (1)	P_T $T_A = +25^\circ\text{C}$ (free Air)	$R_{\theta JC}$ (2)	V_{DS}	V_{GS}	I_{D1} $T_C =$ $+25^\circ\text{C}$ (3)	I_{D2} $T_C =$ $+100^\circ\text{C}$ (3)	I_D Pulse	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>
2N7678UFGC	81	2.78	1.55	40	-4, +6	90	57	477	-55
2N7679UFDC	66	2.78	1.89	40	-4, +6	81	51	477	to
2N7680UFGC	81	2.23	1.55	100	-4, +6	90	57	310	+150
2N7681UFGC	81	1.47	1.55	200	-4, +6	76	48	153	

- (1) Derate linearly by 0.65 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$ for 2N7678, 2N7680 and 2N7681 and 0.53 W/ $^\circ\text{C}$ for 2N7679.
- (2) See [figure 4](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit: I_D may be limited by package.
- (4) Single pulse Drain Current with a $t_{\text{pulse}} \leq 80 \mu\text{s}$.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) * (r_{DS(on)} \text{ at } T_{JM})}}$$

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FSC 5961

MIL-PRF-19500/787

1.4 Primary electrical characteristics. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type (1)	V _{DS} rated	V _{GS} (th)1	Max I _{DSS1}	Max r _{DS(on)} (1) V _{GS} = 5.0 V dc I _{D1}		Max Dr _{DS(on)} V _{GS} =5.0 V (2)
		V _{DS} = V _{GS} I _D = 5 mA dc	V _{GS} = 0 V V _{DS} = 100% rated V _{DS}	T _J = +25°C	T _J = +125°C	T _J = +25°C V _{DS(off)} = V _{DS} rated
	<u>V dc</u>	<u>V dc</u> <u>Min</u> <u>Max</u>	<u>μA dc</u>	<u>Ohm</u>	<u>Ohm</u>	<u>Ohm</u>
2N7678UFGC	40	0.8 2.5	530	0.0045	0.008	0.0052
2N7679UFDC	40	0.8 2.5	530	0.0050	0.009	0.0058
2N7680UFGC	100	0.8 2.5	345	0.0060	0.010	0.0069
2N7681UFGC	200	0.8 2.5	200	0.0145	0.026	0.0167

(1) Pulsed (see 4.5.1).

(2) According to JEP173 within 10us.

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTX", "JANTXV" and "JANS".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANH C" and "JANKC".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7678" and "7679", and "7680" and "7681".

1.5.4.3 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

UFGC	Indicates a 5 pad surface mount package with ceramic lid.
UFDC	Indicates a 4 pad surface mount package with ceramic lid.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A".

1.6 Radiation features The following radiation features are applicable for RHA devices supplied to this specification sheet.

1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of [MIL-STD-750](#) are as follows:

For device type 2N7678UFGC, 2N7679UFDC, 2N7680UFGC 2N7681UFGC: 1 Mrad(Si) 1/

1.6.2 Heavy ion irradiation SEE. SEE testing includes Single-Event Burnout (SEB), Single-Event Dielectric Rupture (SEDR), and Single-Event Gate Rupture (SEGR) tests at the specified linear energy transfer (LET) units. See [6.7](#) for the specific RHA SEE characterization testing details. The following characterization conditions were used for the testing to the requirements herein:

For device types 2N7678UFGC, 2N7679UFDC, 2N7680UFGC 2N7681UFGC:

No SEB, SEDR, and SEGR were observed at surface LET (see table IV) ≤ 84.6 MeV·cm²/mg (Si) 2/

(In-situ bias conditions: VDS = 40 V and VGS = -4 V)

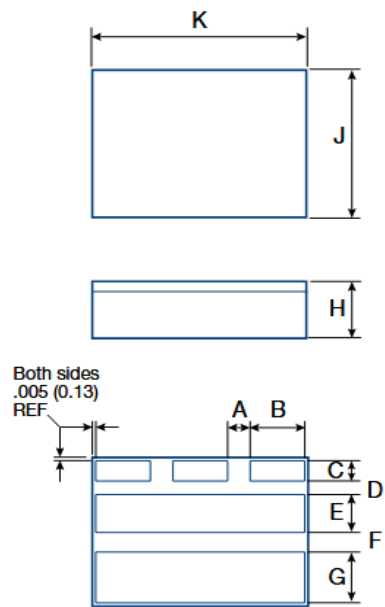
(In-situ bias conditions: VDS = 40 V and VGS = -4 V)

(In-situ bias conditions: VDS = 100 V and VGS = -4 V)

(In-situ bias conditions: VDS = 150 V and VGS = -4 V)

1/ Manufacturer supplying these device types have performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 1 Mrad(Si). The test is performed per wafer lot on 10 devices per bias.

2/ Manufacturer also performed heavy ion SEB, SEDR, and SEGR test at Texas A&M University (TAMU) Radiation Effects Facility in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEDR/SEGR) characteristics. This test is performed on every wafer fabrication lot. For more information on SEE (SEB/SEDR/SEGR) test results, customers are requested to contact the manufacturer.

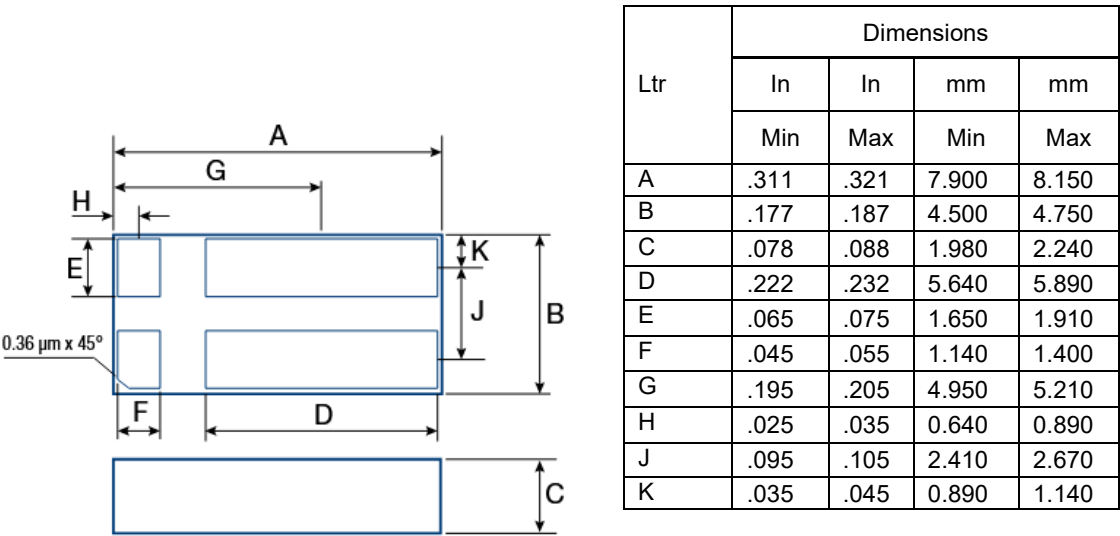


Ltr	Dimensions			
	In	In	mm	mm
	Min	Max	Min	Max
A	.028	.038	0.711	0.965
B	.075	.085	1.905	2.159
C	.025	.035	0.635	0.889
D	.015	.025	0.381	0.635
E	.051	.061	1.295	1.549
F	.024	.034	0.610	0.864
G	.070	.080	1.778	2.032
H	.078	.088	1.981	2.235
J	.215	.225	5.461	5.715
K	.311	.321	7.899	8.153

UFG Package

- NOTES:
- 1. Dimensions are in inches. Millimeters are given for general information only.
 - 2. Package thickness dimensions are pre solder dip.

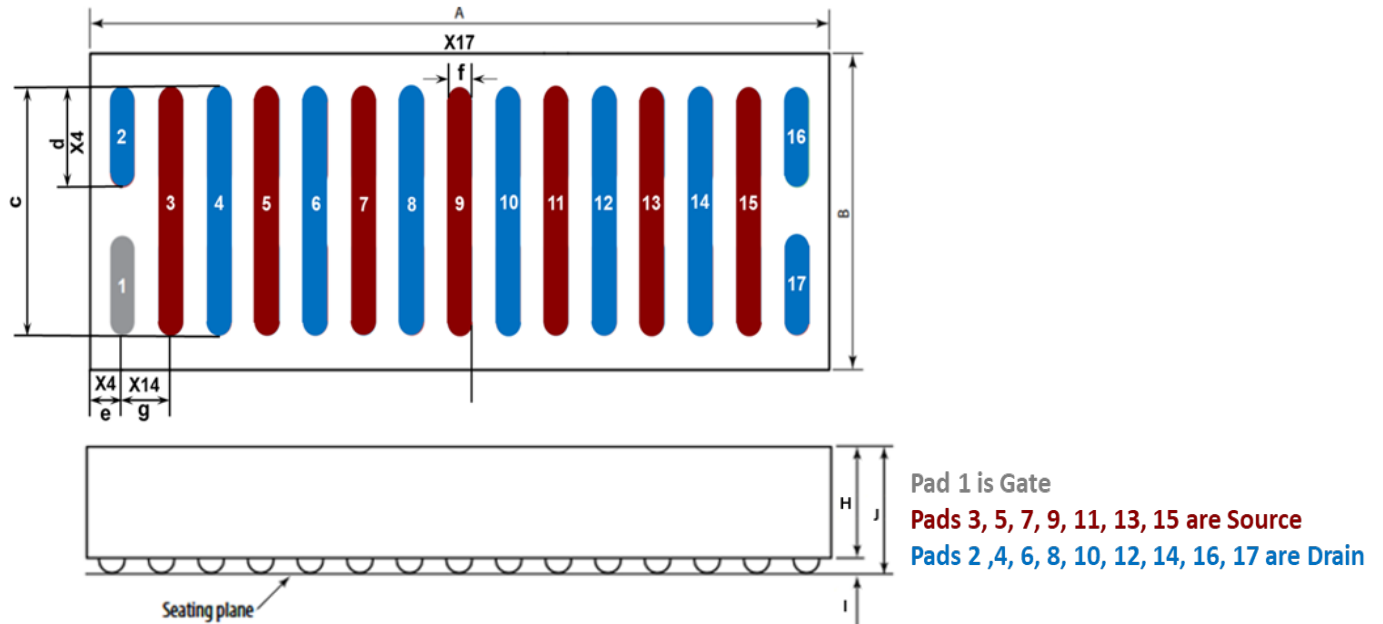
FIGURE 1. Physical dimensions, surface mount UFG.



UFD Package

- NOTES:
- 1. Dimensions are in inches. Millimeters are given for general information only.
 - 2. Package thickness dimensions are pre solder dip.

FIGURE 2. Physical dimensions, surface mount UFD.

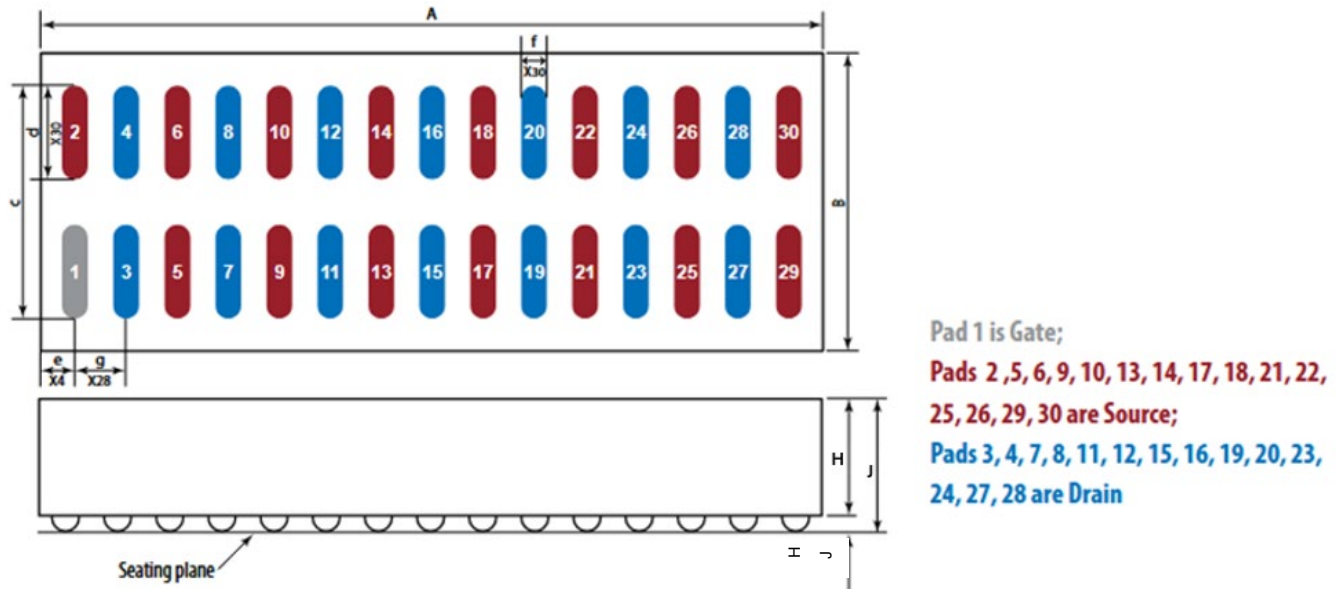


Ltr	Dimensions					
	in	in	in	mm	mm	mm
	Min	Nom	Max	Min	Nom	Max
A	0.237	0.238	0.239	6.020	6.050	6.080
B	0.089	0.091	0.092	2.270	2.300	2.330
C	0.069	0.069	0.069	1.747	1.750	1.753
D	0.026	0.026	0.026	0.657	0.660	0.663
E	0.008	0.009	0.009	0.210	0.225	0.240
F	0.008	0.008	0.008	0.195	0.200	0.205
G	0.016	0.016	0.016	0.400	0.400	0.400
H		0.027			0.685	
I	0.003	0.003	0.004	0.069	0.087	0.105
J			0.031			0.785

NOTES:

1. Top metal: 87 μ m nominal 95Pb5Sn bump on top of 4 μ m nominal of Aluminum.
2. Back metal: N/A
3. Substrate pad should be connected to source.

FIGURE 3. Physical dimensions JANHCA and JANKCA 2N7678 and 2N7679 version die dimensions.



Ltr	Dimensions –					
	in	in	in	mm	mm	mm
	Min	Nom	Max	Min	Nom	Max
A	0.237	0.238	0.239	6.020	6.050	6.080
B	0.089	0.091	0.092	2.270	2.300	2.330
c	0.081	0.081	0.081	2.047	2.050	2.053
d	0.028	0.028	0.028	0.717	0.720	0.723
e	0.008	0.009	0.009	0.210	0.225	0.240
f	0.008	0.008	0.008	0.195	0.200	0.205
g	0.016	0.016	0.016	0.400	0.400	0.400
H		0.027			0.685	
I	0.003	0.003	0.004	0.069	0.087	0.105
J			0.031			0.785

NOTES:

1. Top metal: 87 μm nominal 95Pb5Sn bump on top of 4 μm nominal of Aluminum.
2. Back metal: N/A
3. Substrate pad should be connected to source.

FIGURE 4. Physical dimensions JANHCA and JANKCA 2N7680 version die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

n Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC - SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP138 - User Guidelines for IR Thermal Imaging Determination of Die Temperature
- JEP173 - Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices.
- JEP180 - GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES
- JEP186 - Guideline to Specify a Transient Off-State Withstand Voltage Robustness Indicator in Datasheets for Lateral GaN Power Conversion Devices

(Copies of these documents are available online at <https://www.jedec.org> or from JEDEC - Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington VA 22201-2107)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see [4.2](#) and [6.3](#)).

n Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

GaN.....Gallium Nitride
HEMT.....High Electron Mobility Transistor
nC nano Coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and [figure 1](#) (UFG), [figure 2](#) (UFD), [figure 3](#) (JANHC and JANKC version A for 2N7678 and 2N7679), [figure 4](#) (JANHC and JANKC version A for 2N7680), herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Multiple chip construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#). Marking on the UF package shall consist of an abbreviated part number, the date code, and the manufacturer's symbol or logo. The prefixes JANTX, JANTXV and JANS can be abbreviated as JX, JV, and JS respectively. The "2N" prefix and the "UF" suffix can also be omitted. The radiation hardened designator H, shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, in HEMT areas.
- f. Maintain relative humidity above 30 percent if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#) herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. SEE shall be performed at initial qualification, on every wafer fabrication lot, and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II, except $r_{DS(on)}$ and V_{SD} may be omitted. 1/ SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

4.2.1.2 SEE wafer lot testing. SEE testing on subsequent wafer fabrication lots shall be tested using a minimum of the ion with the highest surface LET (3 samples for each wafer lot) until sufficient data is collected and approved by the qualifying activity.

1/ SEE testing of this design requires mounting bare die on a coupon face up and wire bonding the solder bumps with one mil gold wire. $r_{DS(on)}$ and V_{SD} cannot be tested through 1 mil wire at rated currents.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANS	Measurements for JANTX and JANTXV
4	Method 2006 of MIL-STD-750	
5	Method 2052 of MIL-STD-750	
7	Method 1071 of MIL-STD-750	
9	Subgroup 2 of table I herein I_{DSS1} , I_{GSSF1} , I_{GSSR1} as minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11 (1)	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 300 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 30 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 15 \mu A$ dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13 (1)	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 300 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 30 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 15 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 33$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 700$ mV dc or ± 30 percent of initial value.	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 300 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 30 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 15 \mu A$ dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 33$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 700$ mV dc or ± 30 percent of initial value.
14	Dynamic $r_{DS(on)}$ JEP173 Double Pulse, see 4.5.2	
15	Method 1071 of MIL-STD-750, a. test condition A b. fine leak	Method 1071 of MIL-STD-750, a. test condition A b. fine leak
16	Method 2076 of MIL-STD-750, See 4.5.3	Method 2076 of MIL-STD-750, See 4.5.3
17	Subgroup 2 of table I herein	
18	Method 2071 of MIL-STD-750	

(1) Devices containing a gate without an oxide layer may omit deltas in the negative direction from the PDA.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTX, JANTXV) of [MIL-PRF-19500](#), and herein.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B4	1042	Intermittent operation life, condition D, $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated } V_{GS}$; $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated } V_{DS}$; $T_A = +150^\circ\text{C}$, $t = 240$ hours minimum.
B5	2037	Not applicable.

4.4.2.2 Quality levels JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition C, 25 cycles.
B3	1042	Intermittent operation life, condition D. $t_{on} = 30$ seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength is not applicable.
C2	2017	Die Shear / Die Pull. 6 devices. May be eliminated when sufficient data is collected and approved by qualifying activity.
C6	1042	Intermittent operation life, condition D. $t_{on} = 30$ seconds minimum.
C6	2037	Not applicable.
C6	2017	Die Shear / Die Pull. 6 devices. May be eliminated when sufficient data is collected and approved by qualifying activity.

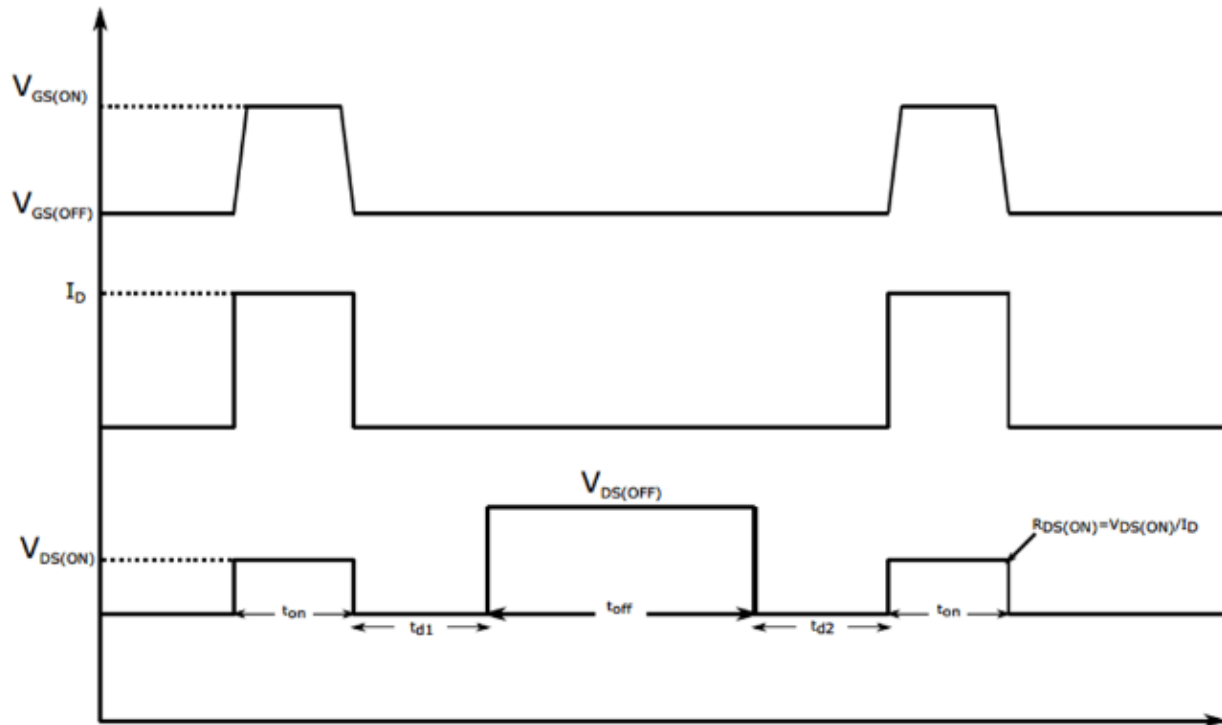
4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Dynamic $R_{DS(on)}$. The $D_{rDS(on)}$ is performed according to the Pulse Current Voltage method in JEP173. $V_{GS} = 5.0$ V, $V_{DS-stress} = 80$ percent rated, Stress time = 10 s, t_{on} is determined by tester configuration and should be short enough to not heat the device. t_{d2} should be less than $10\mu s$ or as fast as possible to avoid trap annealing.



4.5.3 Radiography. Total contact area voids greater than 15 percent of the total intended contact area is rejectable. If 5 percent or more of the devices in a JANS inspection lot fail this die attach criteria, the lot shall be reviewed, and appropriate corrective action taken. Any bridging between conductive paths or more than one bridge within a conductive path is rejectable. In addition, if the die attach image shows any unusual anomalies, the lot shall be reviewed, and appropriate corrective action shall be taken.

4.5.4 Switching dynamic $R_{DS(on)}$. The switching Dynamic $R_{DS(on)}$ is performed within the guidelines of JEP180 in a hard switch test vehicle. The circuit switches a resistive load and monitors $R_{DS(on)}$ during the ON time based on the following criteria:

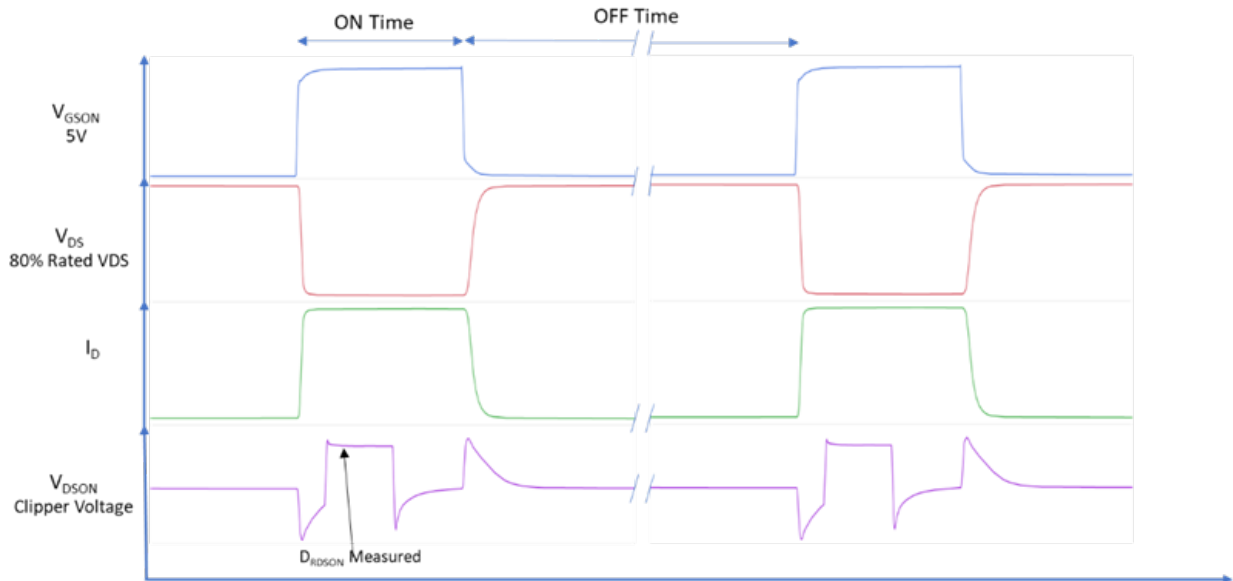
$V_{DS} = 80$ percent of rated voltage

$I_D = 40 - 60$ percent of rated current set by resistive load to properly measure the on-state voltage drop

$T_J = 80^\circ\text{C}$

Duty Cycle = 0.1 percent

Frequency $\geq 500\text{Hz}$



4.5.5 SEE test circuit: When designing the test circuit for the SEE testing, the gate resistance should be kept as low as possible (less than or equal to 1 Ohm) as shown in the circuit below. This is to prevent the gate from turning on during SEE transient.

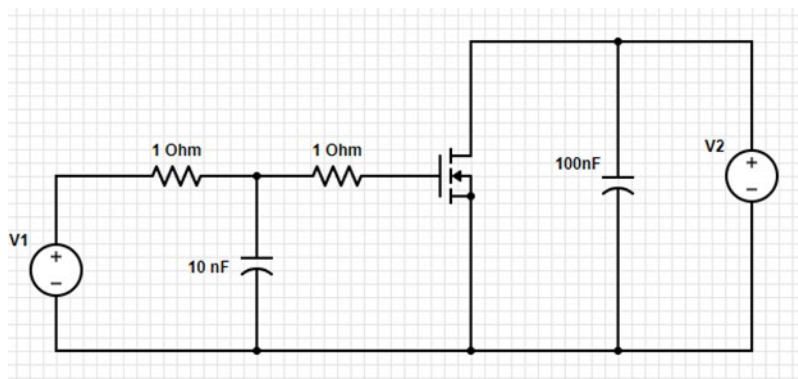


TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750 or industry standard		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 5$ mA dc	$V_{GS(TH)1}$	0.8	2.5	V dc
Gate current	3411	$V_{GS} = +6$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		500	μ A dc
Gate current	3411	$V_{GS} = -4$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}			
2N7678UFGC					-500	μ A dc
2N7679UFDC					-500	μ A dc
2N7680UFGC					-500	μ A dc
2N7681UFGC					-500	μ A dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 100$ percent of rated V_{DS}	I_{DSS1}			
2N7678UFGC					400	μ A dc
2N7679UFDC					400	μ A dc
2N7680UFGC					400	μ A dc
2N7681UFGC					400	μ A dc
Static drain to source on-state resistance	3421	$V_{GS} = 5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(ON)1}$			
2N7678UFGC					0.0045	Ω
2N7679UFDC					0.0050	Ω
2N7680UFGC					0.0060	Ω
2N7681UFGC					0.0145	Ω
Dynamic ON-Resistance <u>2</u> /	JEP173	$V_{GS} = 5.0$ V, $V_{DS-stress} = 80$ percent rated, Stress time = 10 s	DR_{DSON}			
2N7678UFGC					0.0052	Ω
2N7679UFDC					0.0058	Ω
2N7680UFGC					0.0069	Ω
2N7681UFGC					0.0167	Ω
Forward voltage	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = 0.5$ A	V_{SD}		3.0	V (pk)
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	$V_{GS} = +6$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF2}		1	mA dc
Gate current	3411	$V_{GS} = -4$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR2}			
2N7678UFGC					-1	mA dc
2N7679UFDC					-1	mA dc
2N7680UFGC					-1	mA dc
2N7681UFGC					-1	mA dc

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750 or industry standard		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u> – Continued.						
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}			
2N7678UFGC					800	μA dc
2N7679UFDC					800	μA dc
2N7680UFGC					800	μA dc
2N7681UFGC					800	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 5$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(ON)2}$			
2N7678UFGC					0.008	Ω
2N7679UFDC					0.009	Ω
2N7680UFGC					0.010	Ω
2N7681UFGC					0.026	Ω
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 18$ mA dc	$V_{GS(TH)2}$	0.7		V dc
Low temperature operation:		$T_C = T_J = -55^{\circ}C$				
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 18$ mA dc	$V_{GS(TH)3}$		3.0	V dc
<u>Subgroup 4</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{DD} = 50$ percent rated V_{DS}				
Total gate charge			Q_G			
2N7678UFGC					15	nC
2N7679UFDC					22.5	nC
2N7680UFGC					15	nC
2N7681UFGC					25	nC
On gate to source charge			Q_{GS}			
2N7678UFGC					5	nC
2N7679UFDC					7.2	nC
2N7680UFGC					6	nC
2N7681UFGC					10	nC
On gate to drain charge			Q_{GD}			
2N7678UFGC					6	nC
2N7679UFDC					5	nC
2N7680UFGC					6	nC
2N7681UFGC					8	nC

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750 or industry standard		Symbol	Limits	Limits	Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u> – Continued.						
Capacitance	3431	$V_{DS} = 50$ percent rated V_{DS}	C_{ISS}			
Input Capacitance						
2N7678UFGC					2830	pF
2N7679UFDC					3000	pF
2N7680UFGC					2100	pF
2N7681UFGC					2830	pF
Output Capacitance			C_{OSS}			
2N7678UFGC					1660	pF
2N7679UFDC					1900	pF
2N7680UFGC					1050	pF
2N7681UFGC					1700	pF
Reverse Transfer Capacitance			C_{RSS}			
2N7678UFGC					35	pF
2N7679UFDC					21	pF
2N7680UFGC					6	pF
2N7681UFGC					35	pF

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 5 (JANS).

TABLE II. Group D inspection.

Inspection	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
				H	H	H	H	
				Min	Max	Min	Max	
<u>1/</u> <u>2/</u> <u>3/</u>	Method	Conditions						
Subgroup 1 Not applicable								
Subgroup 2		$T_C = + 25^{\circ}\text{C}$						
Steady-state total dose irradiation (V_{GS} bias) <u>4/</u>	1019	Condition A, $V_{GS} = 5\text{ V}$; $V_{DS} = 0$						
Steady-state total dose irradiation (V_{DS} bias) <u>4/</u>	1019	Condition A, $V_{GS} = 0$; $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)						
Steady-state total dose irradiation (No bias) <u>4/</u>	1019	$V_{GS} = V_{DS}$ all shorted						
End-point electricals:								
Gate to source voltage (threshold)	3403	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$ dc	$V_{GS(TH)1}$	0.8	2.5	0.8	2.5	V dc
Gate current	3411	$V_{GS} = +6\text{ V}$ dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		500		500	μA dc
Gate current	3411	$V_{GS} = -4\text{ V}$ dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}					
2N7678UFGC					-500		-500	μA dc
2N7679UFDC					-500		-500	μA dc
2N7680UFGC					-500		-500	μA dc
2N7681UFGC					-500		-500	μA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 100$ percent of rated V_{DS}	I_{DSS1}					
2N7678UFGC					400		400	μA dc
2N7679UFDC					400		400	μA dc
2N7680UFGC					400		400	μA dc
2N7681UFGC					400		400	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 5\text{ V}$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(ON)1}$					
2N7678UFGC					0.0045		0.0045	Ω
2N7679UFDC					0.005		0.005	Ω
2N7680UFGC					0.006		0.006	Ω
2N7681UFGC					0.0145		0.0145	Ω
Forward voltage	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = 0.5\text{ A}$	V_{SD}		3.0		3.0	V (pk)

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750 or industry standard		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2</u> <u>1/</u>			45 devices c = 0
V _{DS} transient	JEP186	10K Transient pulses at 120% rated V _{DS} voltage. T _J = 150°C. This test may be performed at any time prior to lot formation.	
Steady-state gate bias <u>4/</u>	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state reverse bias <u>4/</u>	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			
User Guidelines for IR Thermal Imaging Determination of Die Temperature <u>5/</u>	JEP138	Thermal impedance curve development and/or characterization.	
<u>Subgroup 7</u>			3 devices c = 0
Resistance to soldering heat	2031	Condition I, J, or K	
<u>Subgroup 10</u>			12 devices c = 0
Switching Dynamic Life Test	JEP180	Test conditions shall be derived by the manufacturer. See 4.5.4 .	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 11</u>			
SEE <u>2/</u> <u>3/</u>	1080	See MIL-STD-750 method 1080, 4.5.5 , and 6.2 .	
<u>Subgroup 12</u>			4 devices
Surface Mount Device Package Integrity <u>5/</u>	2039	Twist Bend temp cycle visual, Condition C, F, T (4 devices each condition)	

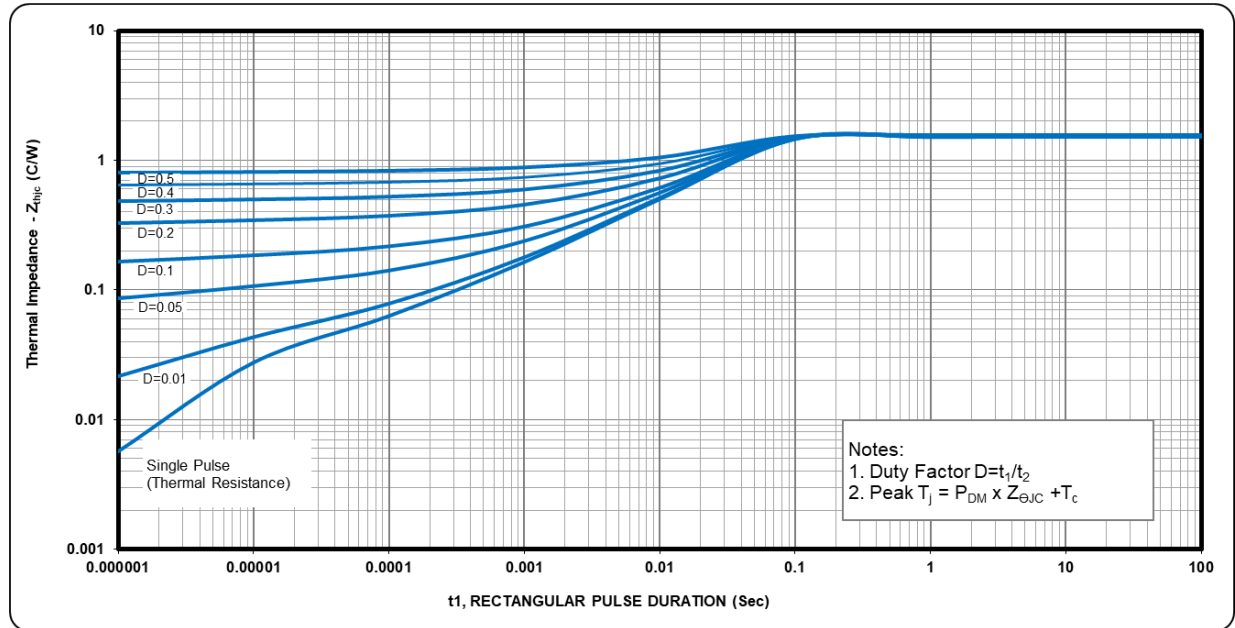
1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE effect testing may be performed prior to lot formation.

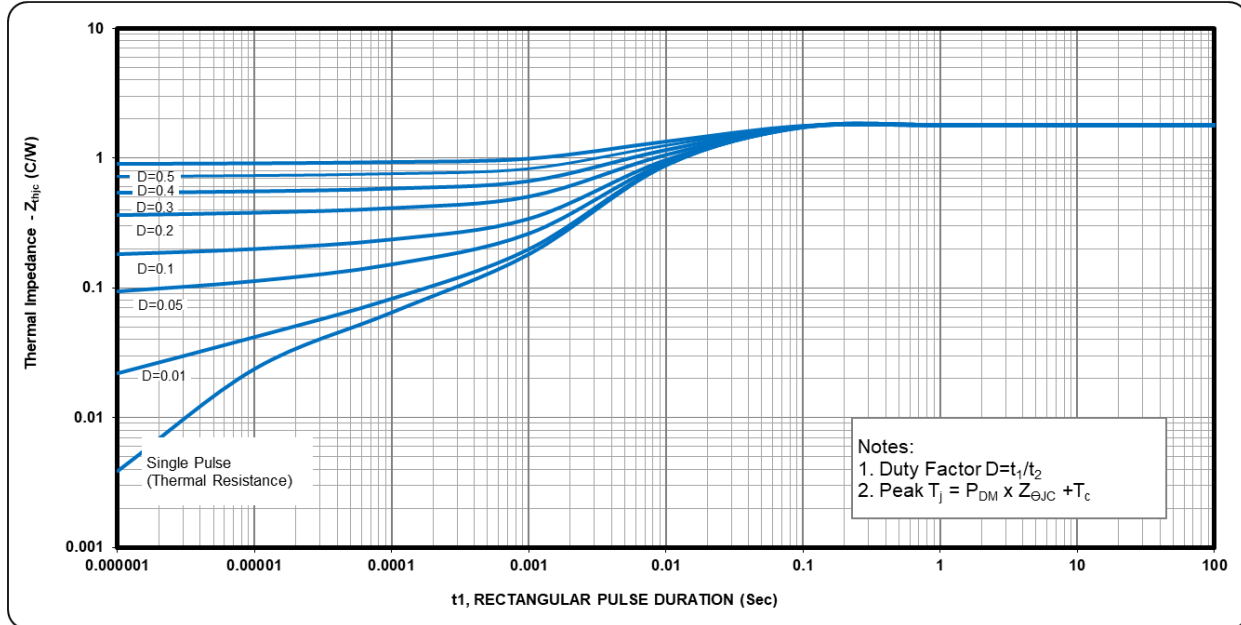
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

4/ For initial qualification perform 2000 hrs and then subsequent Group E testing perform 1000 hrs.

5/ For initial package qualification.



2N7678UFGC, 2N7680UFGC, 2N7681UFGC



2N7679UFDC

FIGURE 5. Thermal impedance graph.

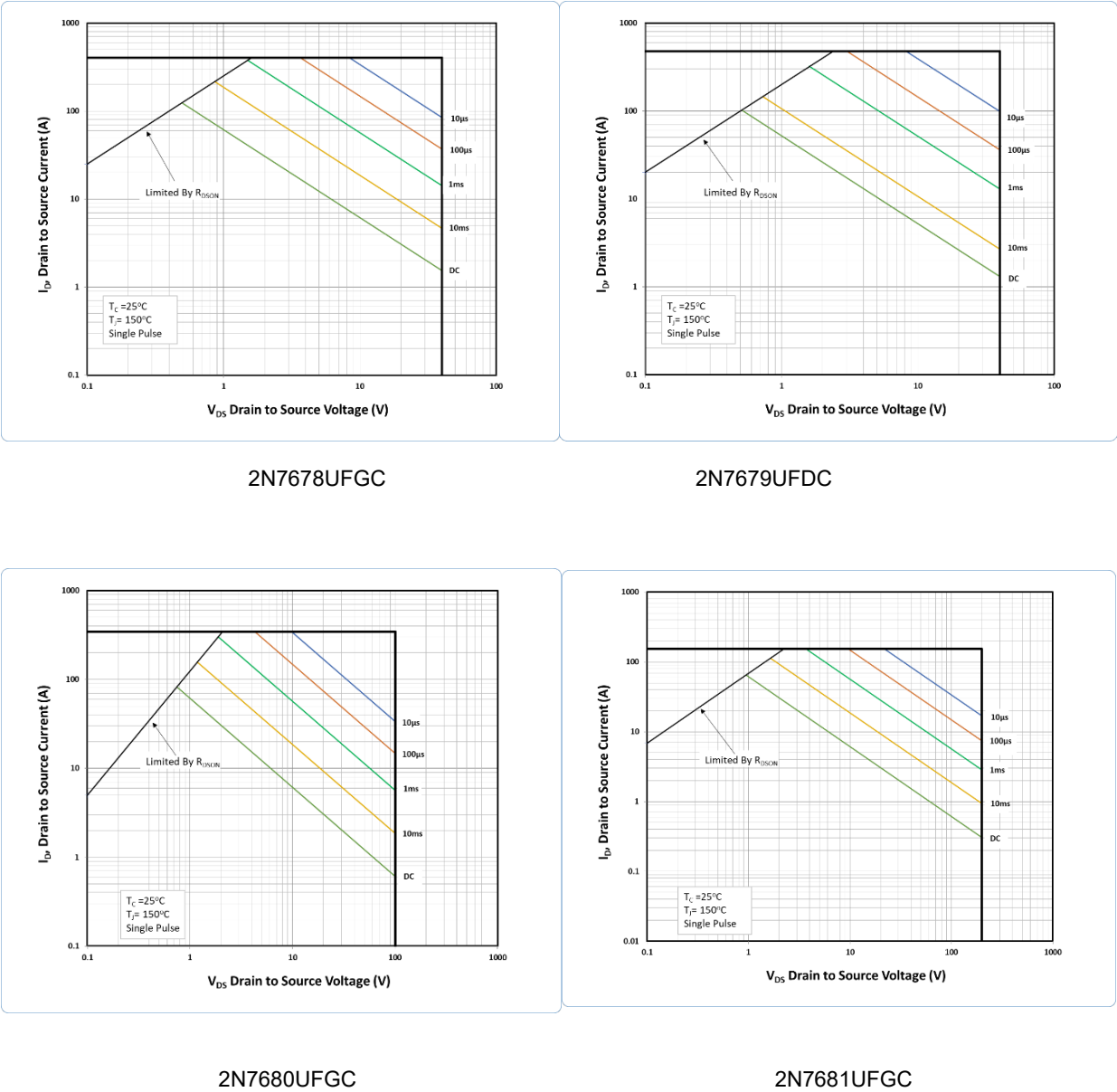


FIGURE 6. Safe-operating-area graph.

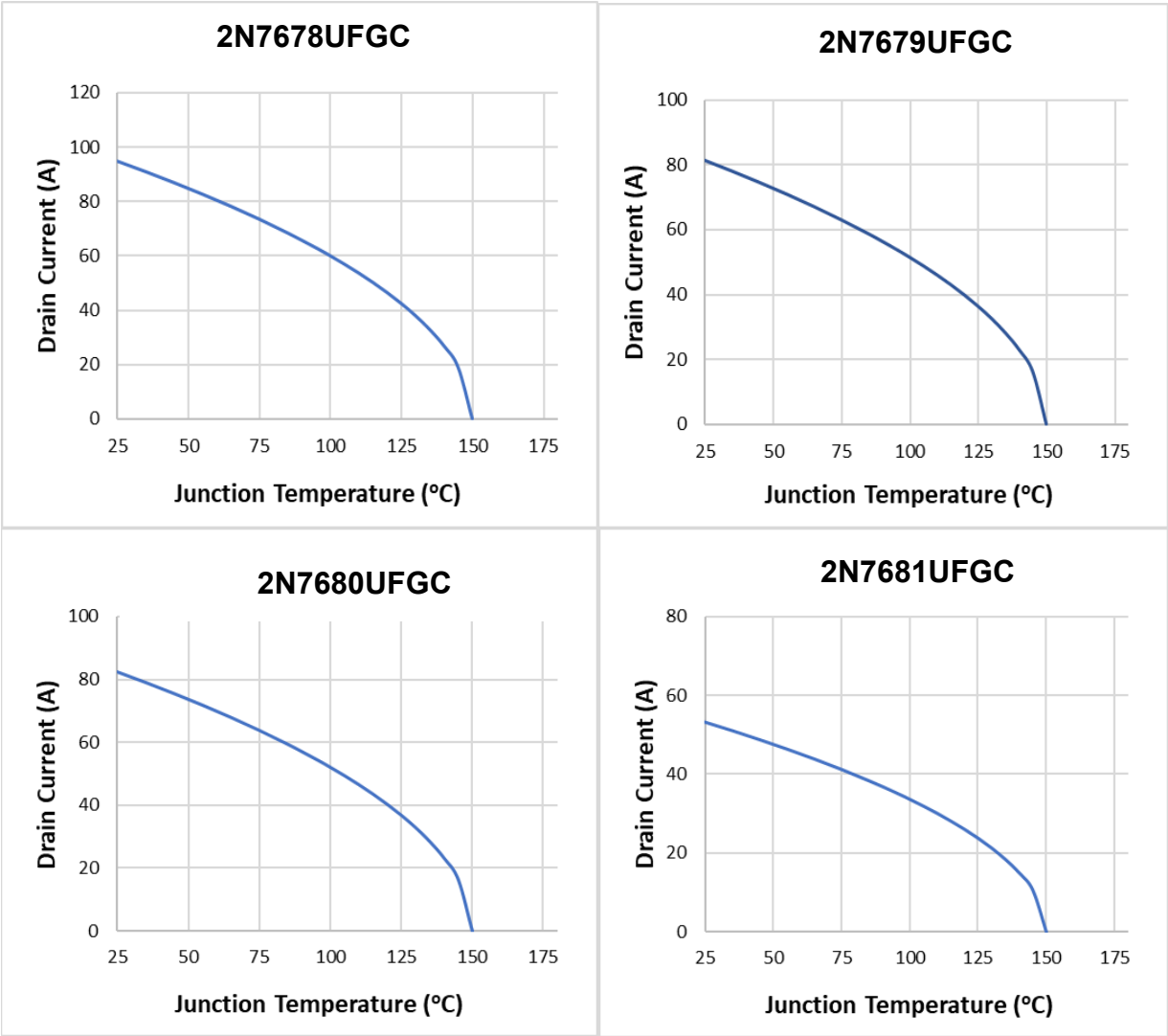


FIGURE 7. Drain Current vs Temperature graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

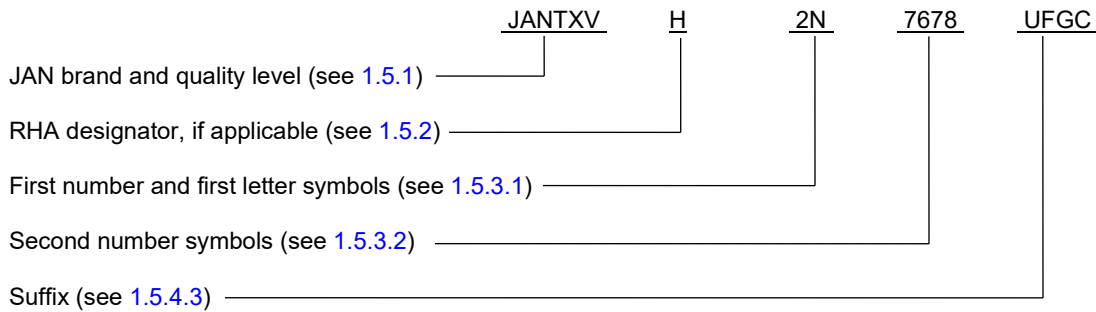
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.
- f. If specific SEE characterization conditions are desired (see section 6.7 and table IV), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs.

6.5.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level with
JANTXH2N7678UFGC	JANTXVH2N7678UFGC	JANSH2N7678UFGC
JANTXH2N7679UFDC	JANTXVH2N7679UFDC	JANSH2N7679UFDC
JANTXH2N7680UFGC	JANTXVH2N7680UFGC	JANSH2N7680UFGC
JANTXH2N7681UFGC	JANTXVH2N7681UFGC	JANSH2N7681UFGC

1/ The M suffix represents a device with a metal lid.

2/ The PIN is also available without an RHA designator.

6.5.2 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

PINs for devices of the "JANHCA" quality level	PINs for devices of the "JANKCA" quality level with
JANHCA2N7678	JANKCA2N7678
JANHCA2N7679	JANKCA2N7679
JANHCA2N7680	JANKCA2N7680
JANHCA2N7681	JANKCA2N7681

6.6 Cross-reference list. The following table shows the manufacture generic P/N and its associated military P/N.

Generic P/N	Military P/N	Package & Termination Configuration
EPC7019G	2N7678UFGC	5-pad, Ceramic Lid
EPC7019D	2N7679UFDC	4-pad, Ceramic Lid
EPC7018G	2N7680UFGC	5-pad, Ceramic Lid
EPC7020G	2N7681UFGC	5-pad, Ceramic Lid

6.7 Application data.

6.7.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection 1/	MIL-STD-750		Sample plan
		Method	Conditions	
8QKQ6	SEE 1/ 2/ Electrical measurements SEE irradiation: 2N7678UFGC 2N7679UFDC 2N7680UFGC 2N7681UFGC Electrical measurements	1080	See MIL-STD-750E method 1080.1 dated 20 November 2006. See figure 7 I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2 Fluence = $1E7$ ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25^{\circ} \pm 5^{\circ}C$ Surface LET = 50 MeV-cm ² /mg (Si) $\pm 5.0\%$, range = $131 \mu m$ (Si) $\pm 7.5\%$, Xe ion energy = 1653 MeV $\pm 7.5\%$ In-situ bias conditions: $V_{DS} = 100\%$ rated, and $V_{GS} = -4$ V Surface LET = 84.6 MeV-cm ² /mg (Si) $\pm 5\%$, range = $130 \mu m$ (Si) $\pm 7.5\%$, Au ion energy = 2482 MeV $\pm 10\%$ In-situ bias conditions: $V_{DS} = 40$ V and $V_{GS} = -4$ V In-situ bias conditions: $V_{DS} = 40$ V and $V_{GS} = -4$ V In-situ bias conditions: $V_{DS} = 100$ V and $V_{GS} = -4$ V In-situ bias conditions: $V_{DS} = 150$ V and $V_{GS} = -4$ V I_{GSSF1} , I_{GSSR1} , and I_{DSS1}	3 devices

1/ I_{GSSF1} , I_{GSSR1} , and I_{DSS1} were examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

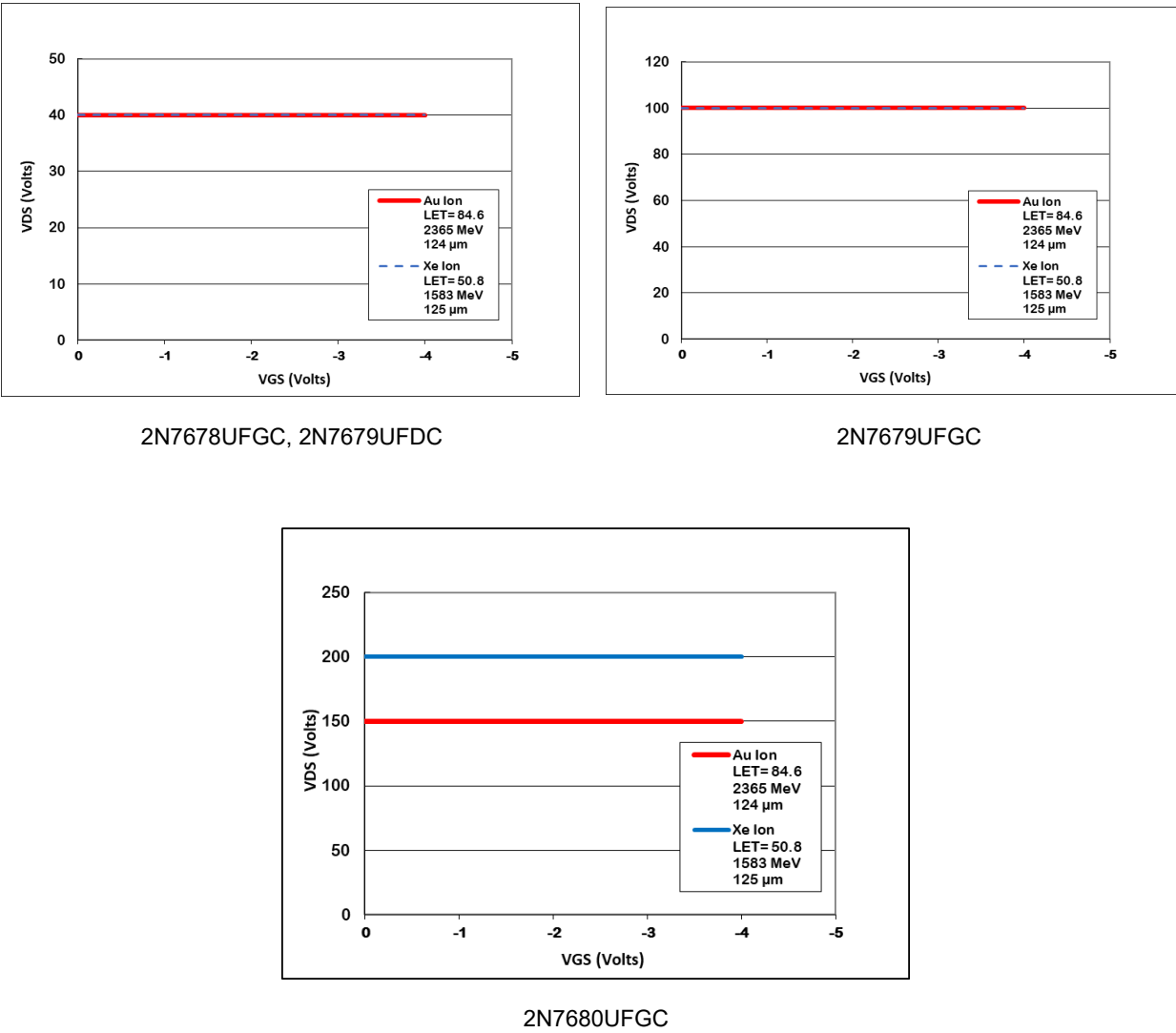


FIGURE 8. Cage 8QKQ6 typical SEE response graph.

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or DSN 850-6939.

Custodians:

Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2024-092)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.